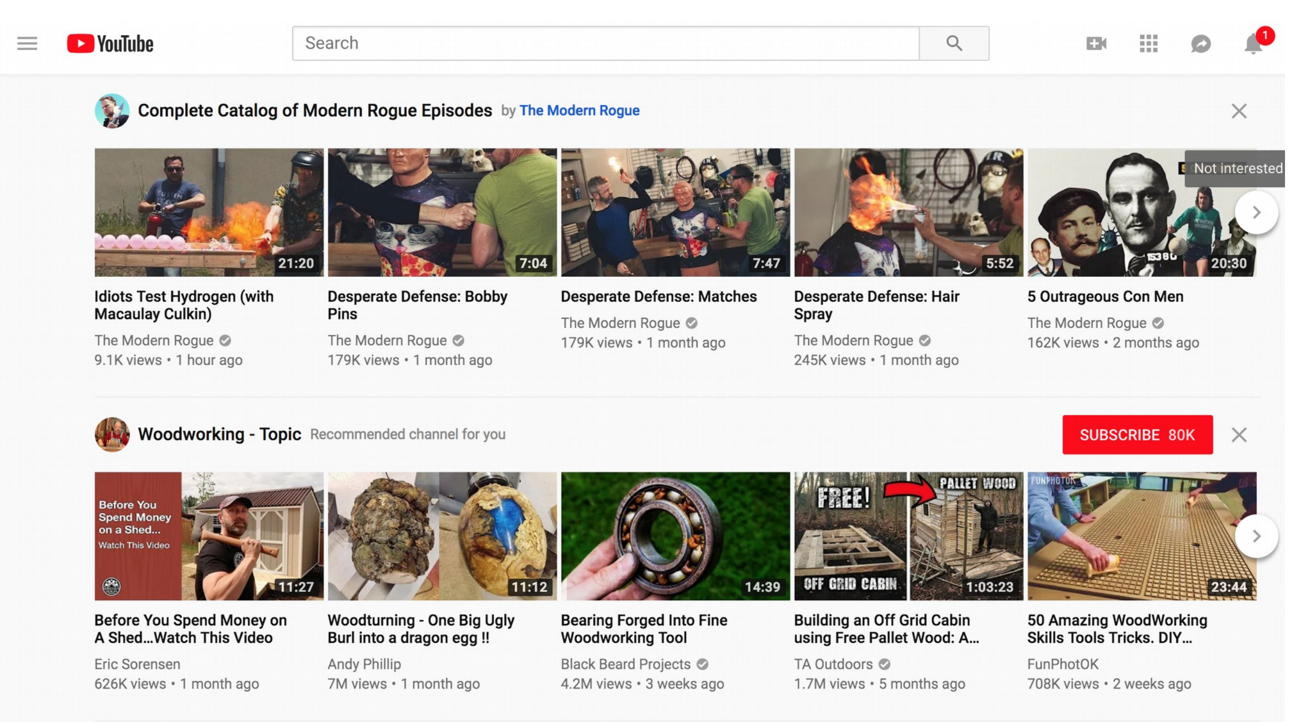
Cross-Stack Characterization and Solid State Drive-Based Near Data Processing for Recommendation Workloads

Samuel Hsia*, **Mark Wilkening***, Udit Gupta,

Caroline Trippel, Carole-Jean Wu, Gu-Yeon Wei, David Brooks

At Boston Area Architecture Workshop (*BARC 2021*)

* Indicates equal contribution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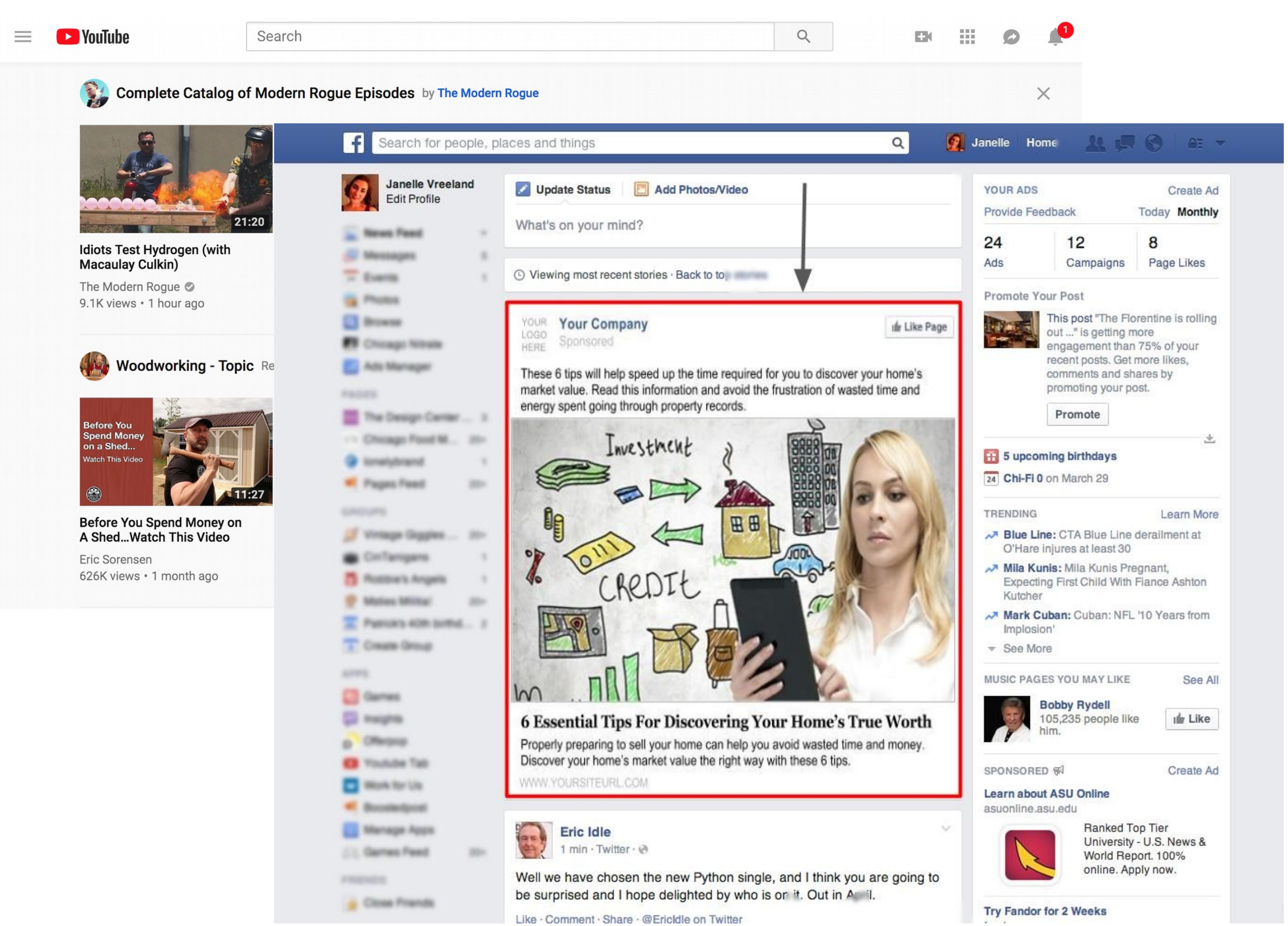
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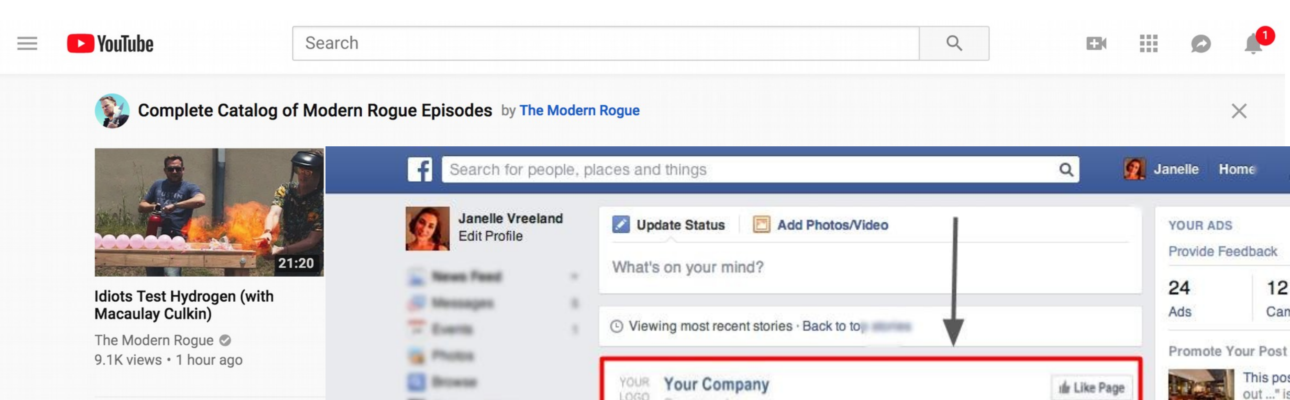
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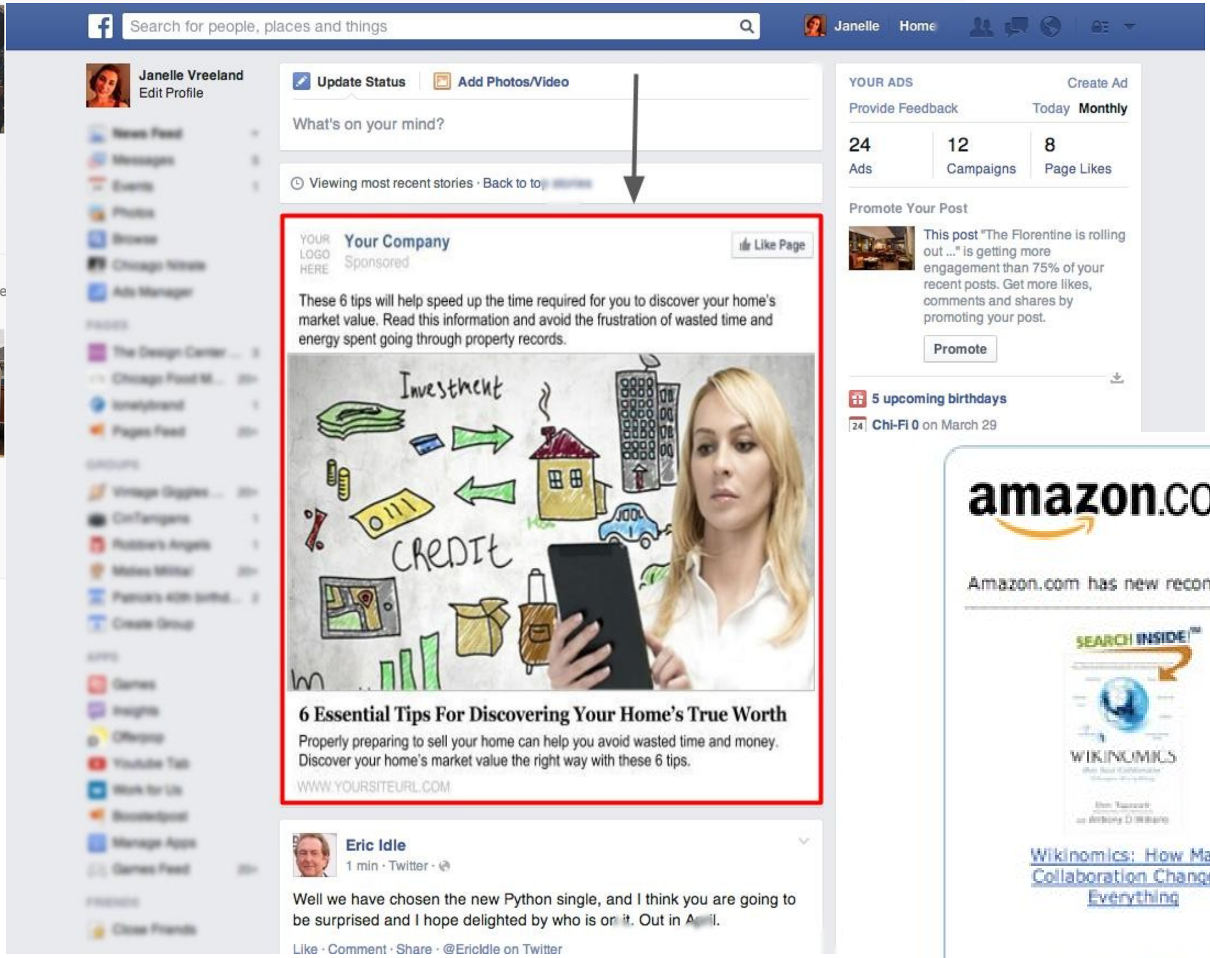
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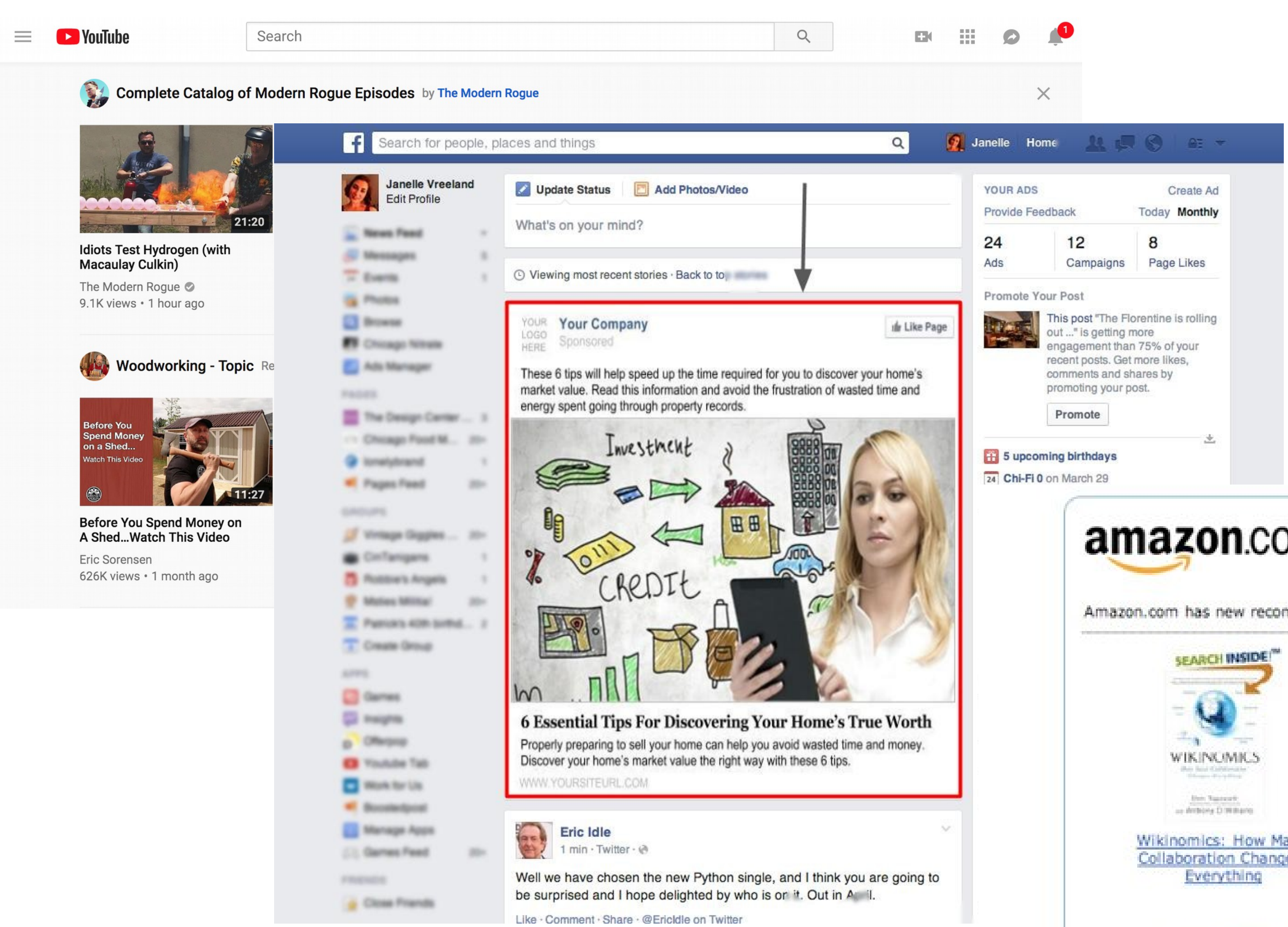
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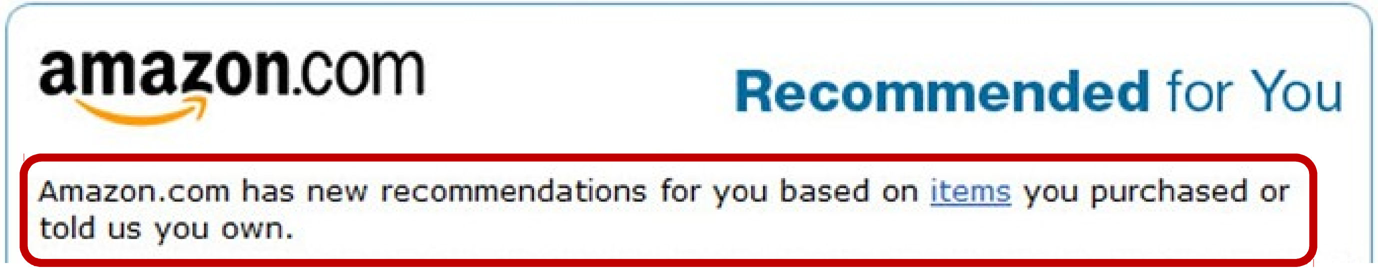
What is recommendation



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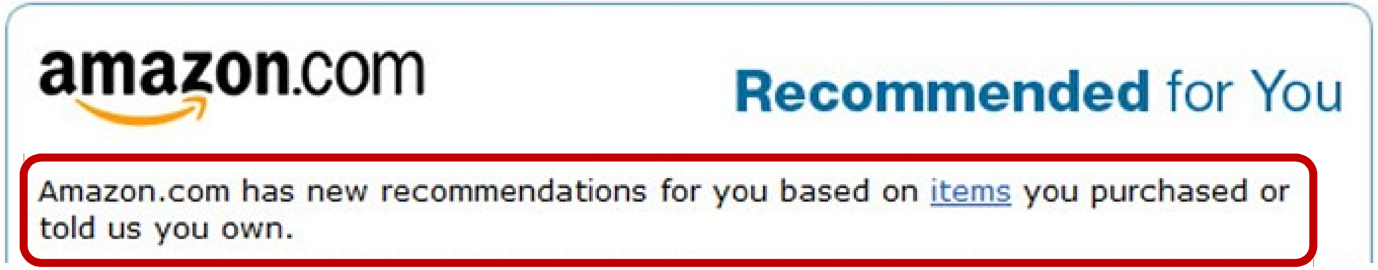
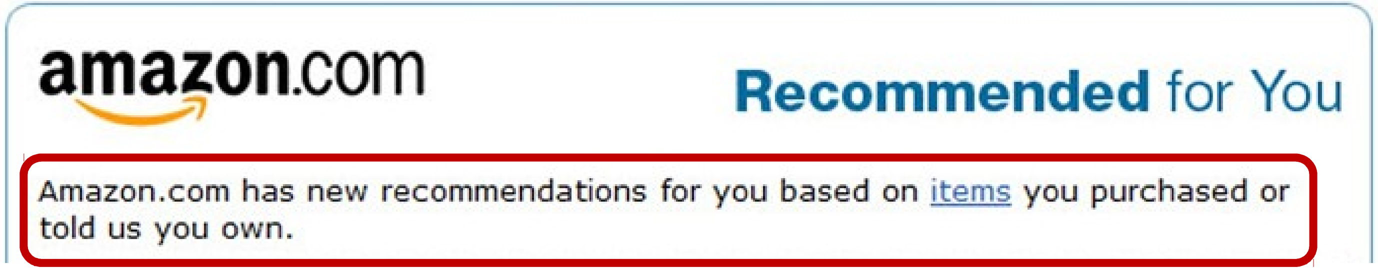
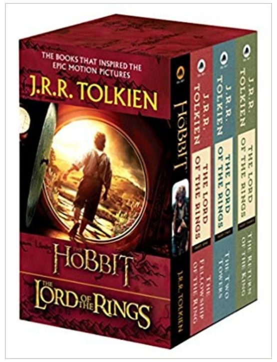


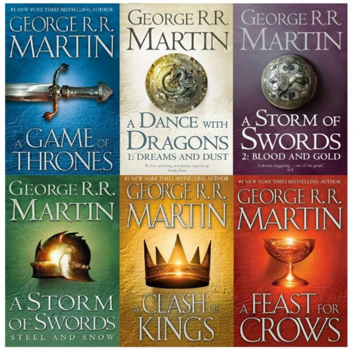
You **Item Preferences**

What is recommendation





Recommendation System

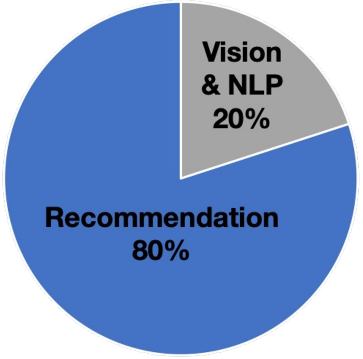


You **Item Preferences** **Item Recommendations**

Why should computer architects care

Why should computer architects care

Infrastructure Demands



Facebook Datacenters' AI Inference Cycles [1]

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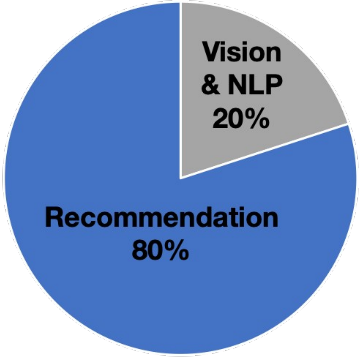

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Also accounts for 50% of training demand [2]

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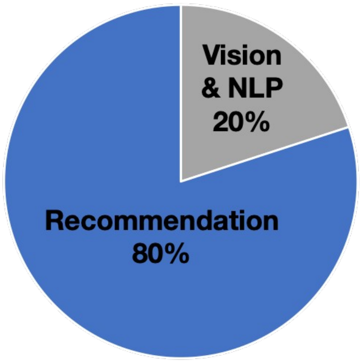

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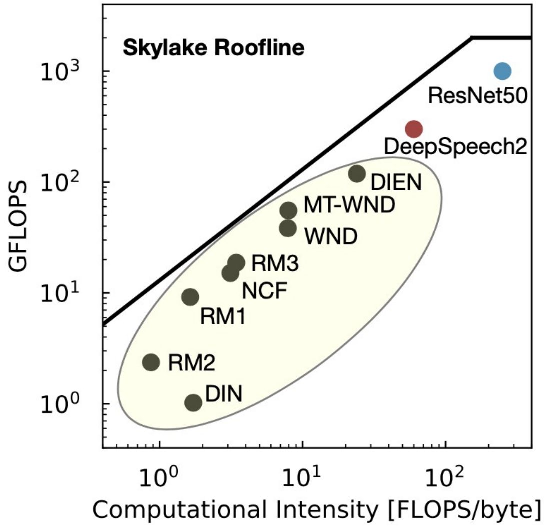
Unique Compute Requirements



Different than CNNs and RNNs

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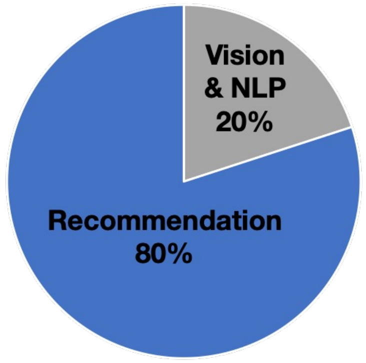

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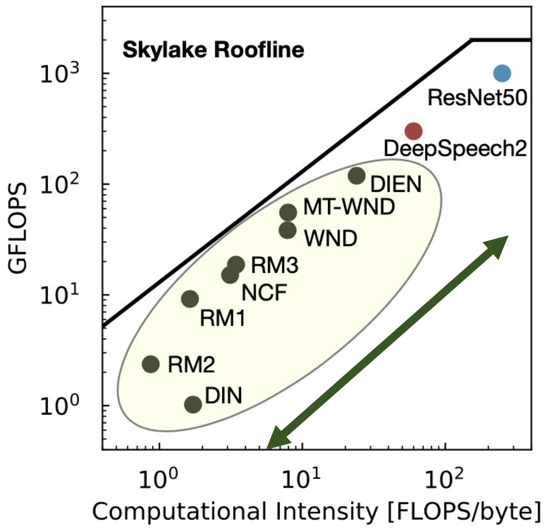

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Model Diversity

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This talk

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Characterization

[IISWC ‘20]

This talk

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RecSSD

[ASPLOS ‘21]

This talk

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Improving recommendation requires **cross-stack characterization**

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Hardware

Recommendation is deployed on **heterogenous hardware**

Improving recommendation requires **cross-stack characterization**

Algorithms	Software	Hardware
 		
Application variety leads to **algorithm diversity**	Algorithms are implemented with **different software frameworks**	Recommendation is deployed on **heterogenous hardware**

Different layers of the execution stack have different bottlenecks!

Characterization

Question: What are the bottlenecks of each layer and how do they affect one another?

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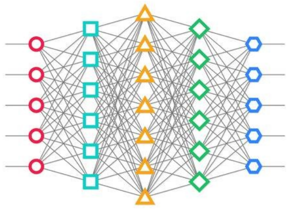

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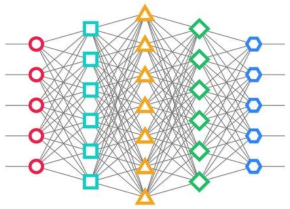

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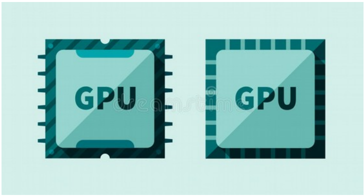

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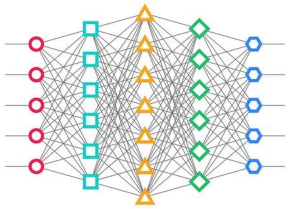

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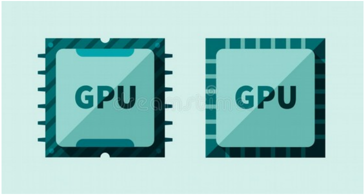

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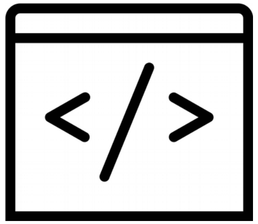

Can we explain the performance trends with **software level operators**?

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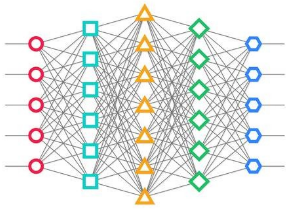

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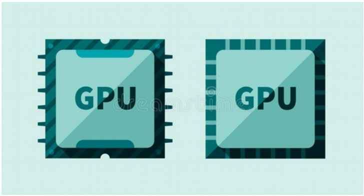

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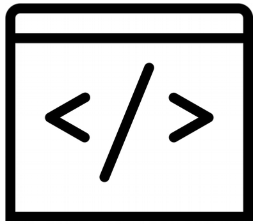

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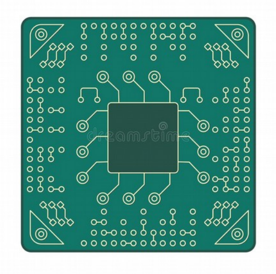

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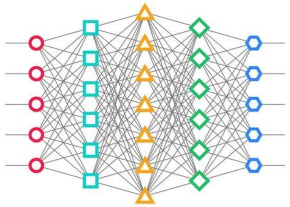

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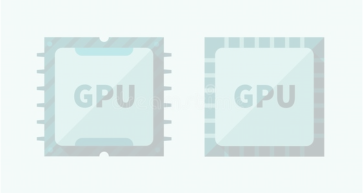

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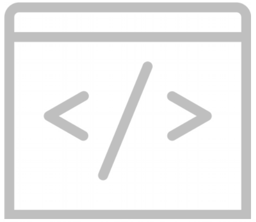

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Deep Recommendation Model Architecture

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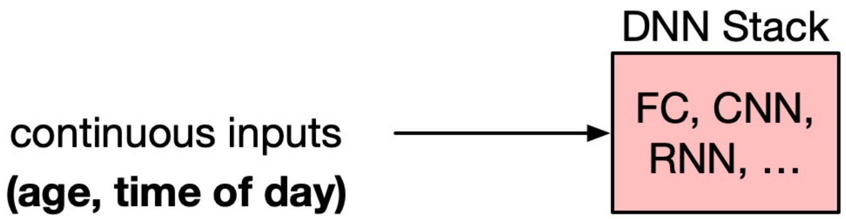

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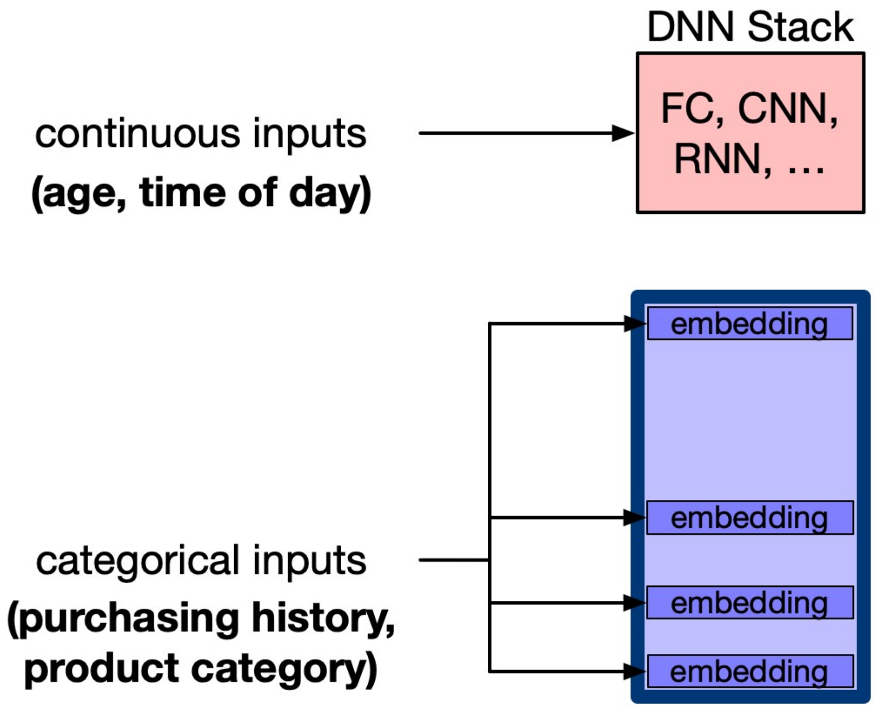

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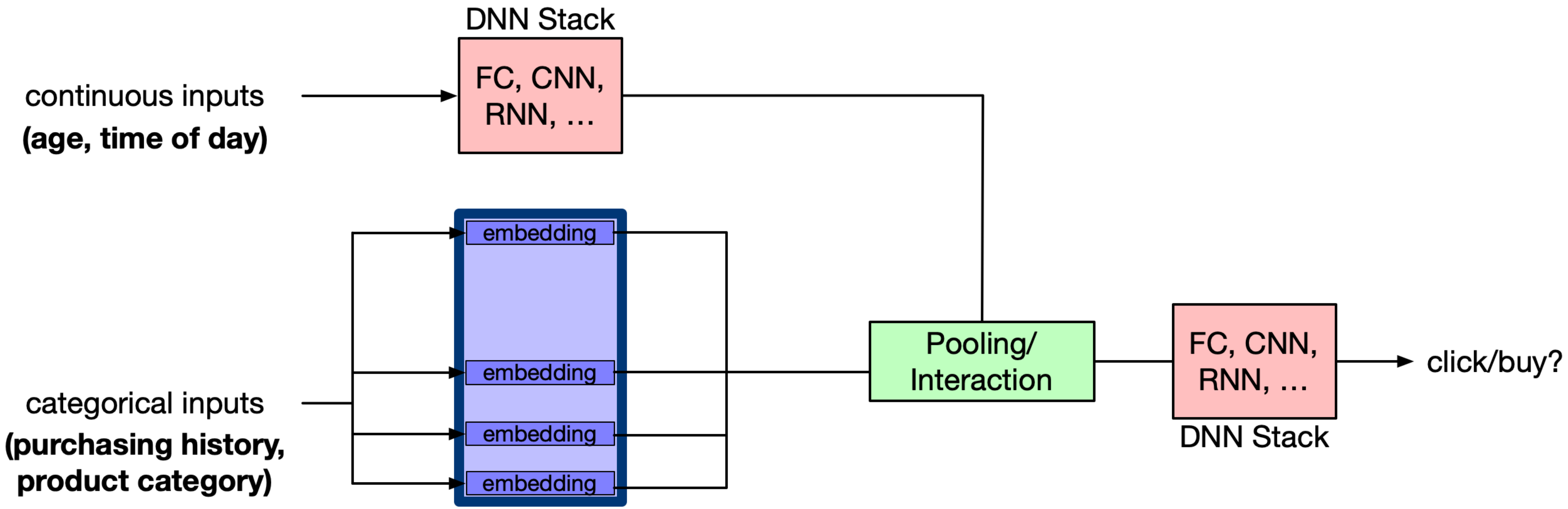

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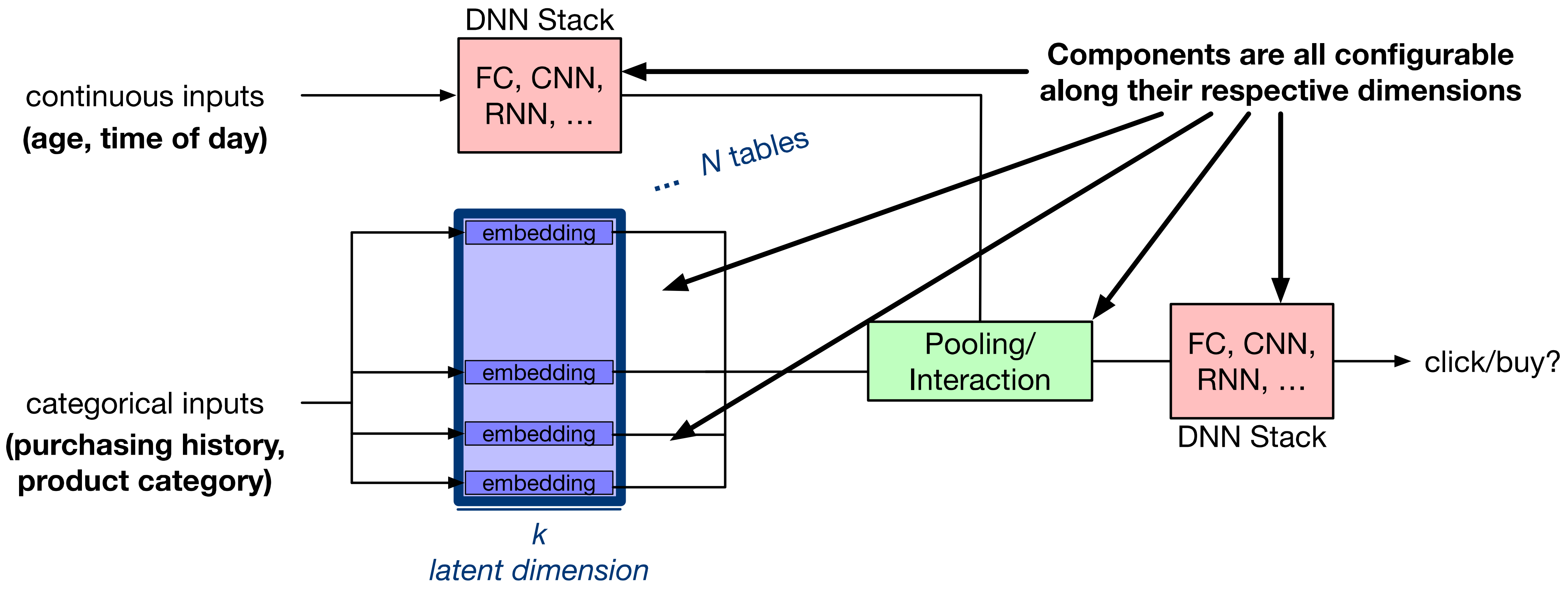

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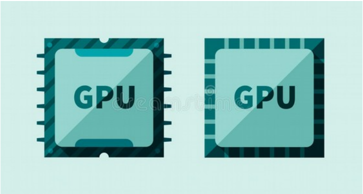

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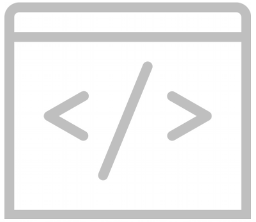

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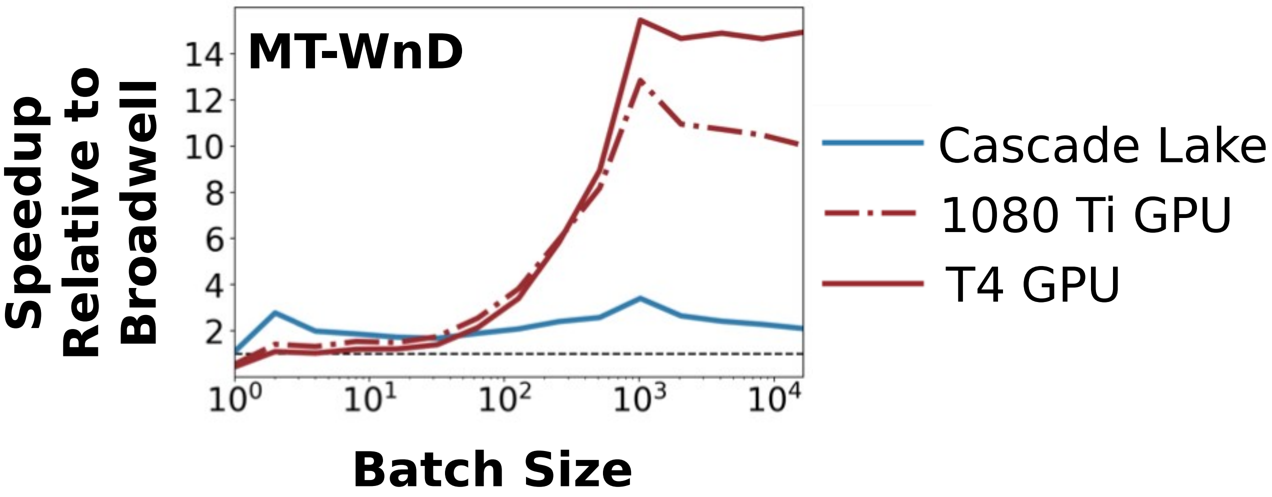

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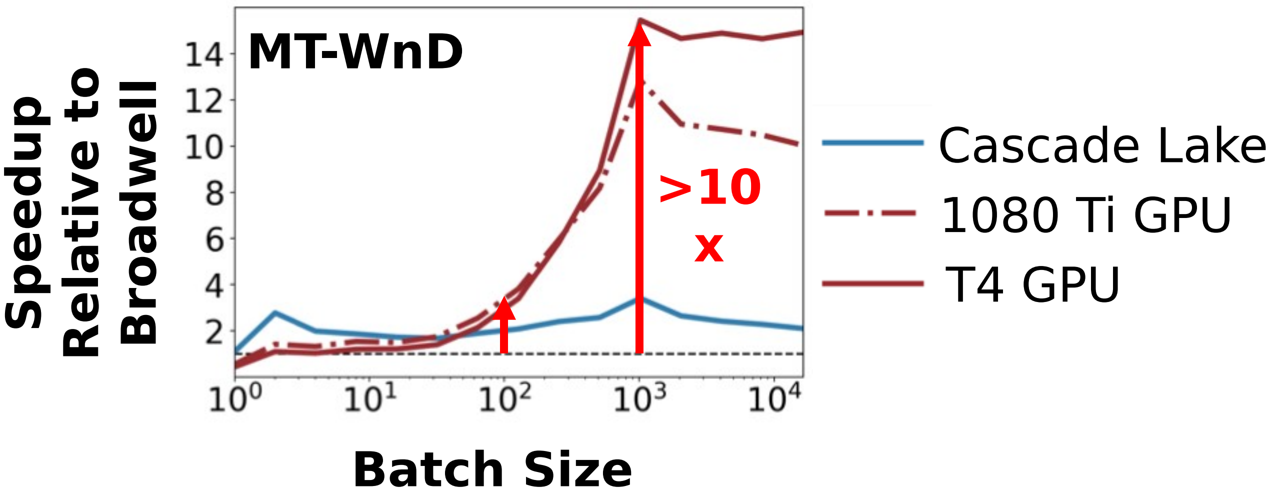
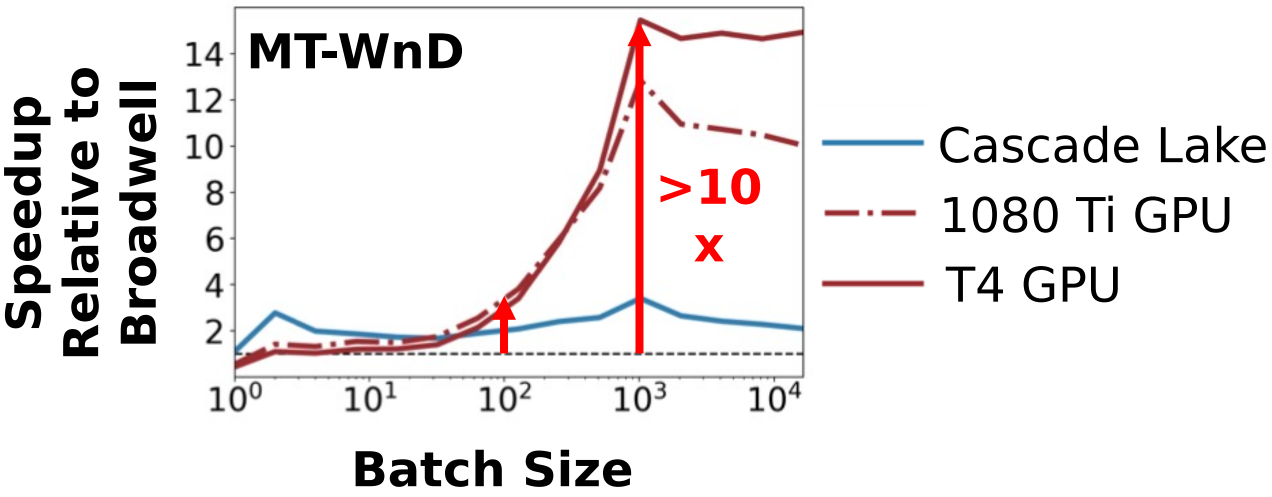


Great speedup on GPUs

Systems Platforms Evaluation



Great speedup on GPUs
Rely on Fully-Connected (FC) stacks

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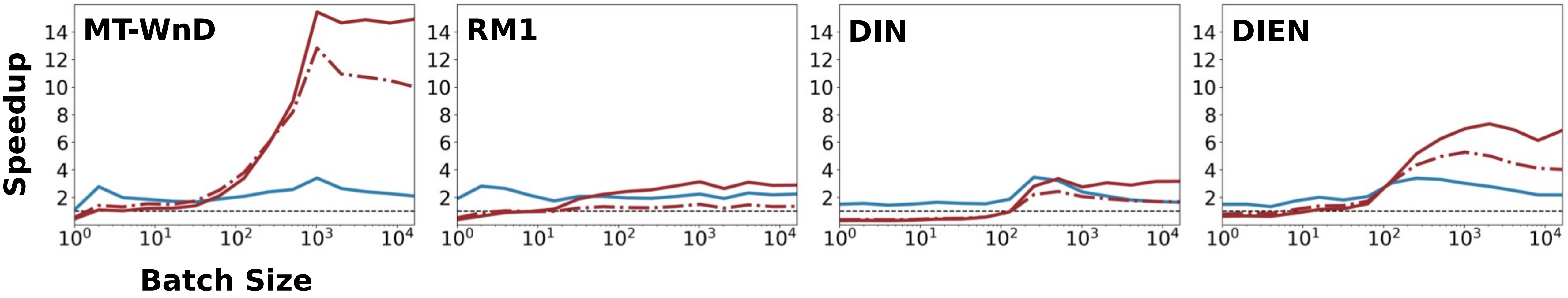


Great speedup on GPUs

Rely on Fully-Connected (FC) stacks

Bad speedup on GPUs

Rely on Embedding lookups

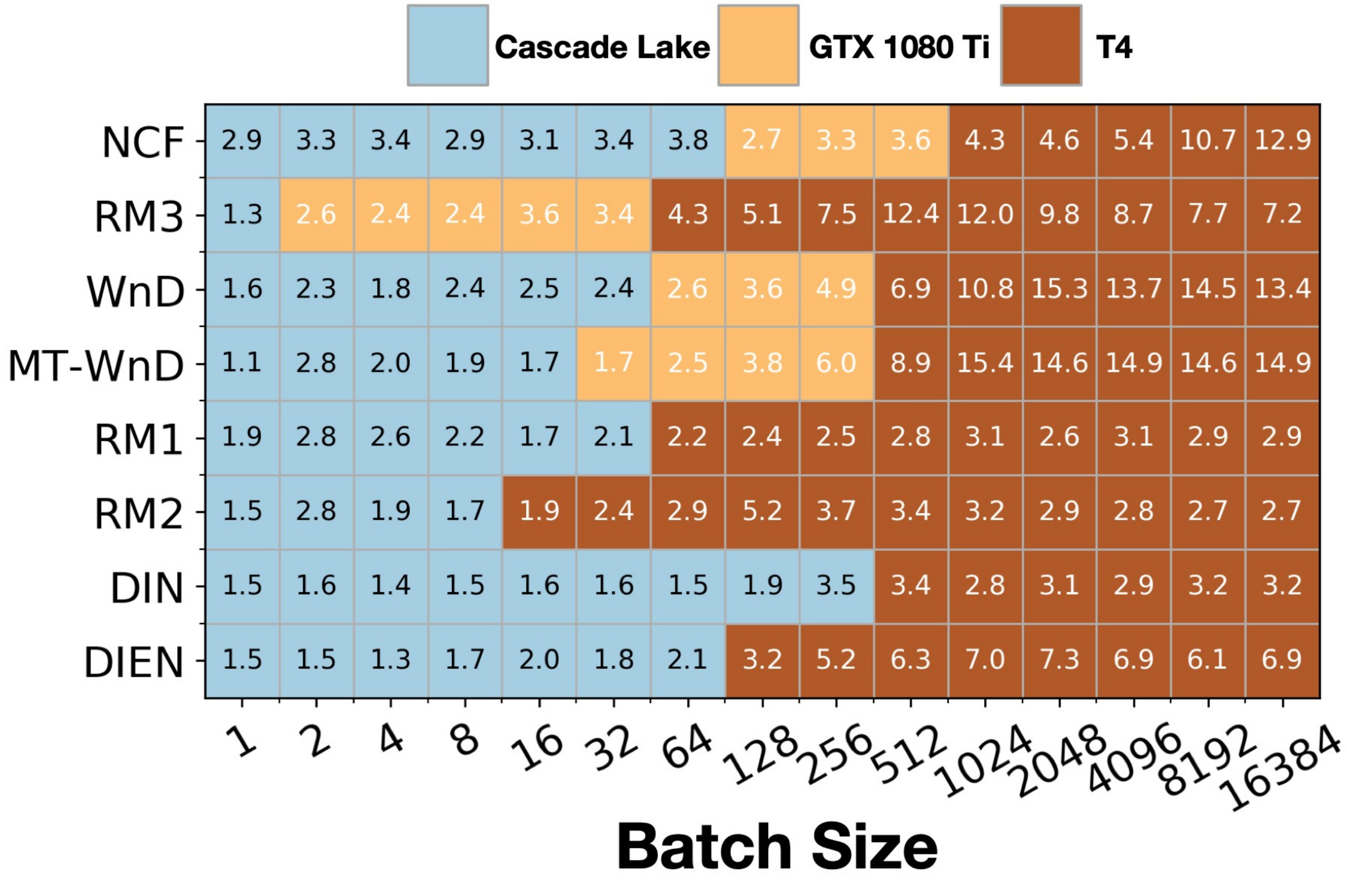
Implements Attention Mechanism

DIN bad on GPUs
DIEN good on GPUs

Cascade Lake
1080 Ti GPU
T4 GPU

Model architecture and use-case play important roles in determining acceleration

Optimal hardware varies based on **model architecture and input batch size**



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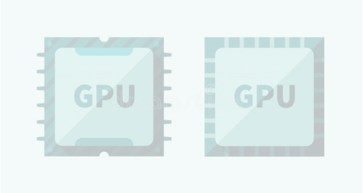

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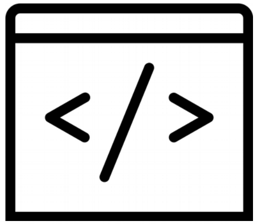
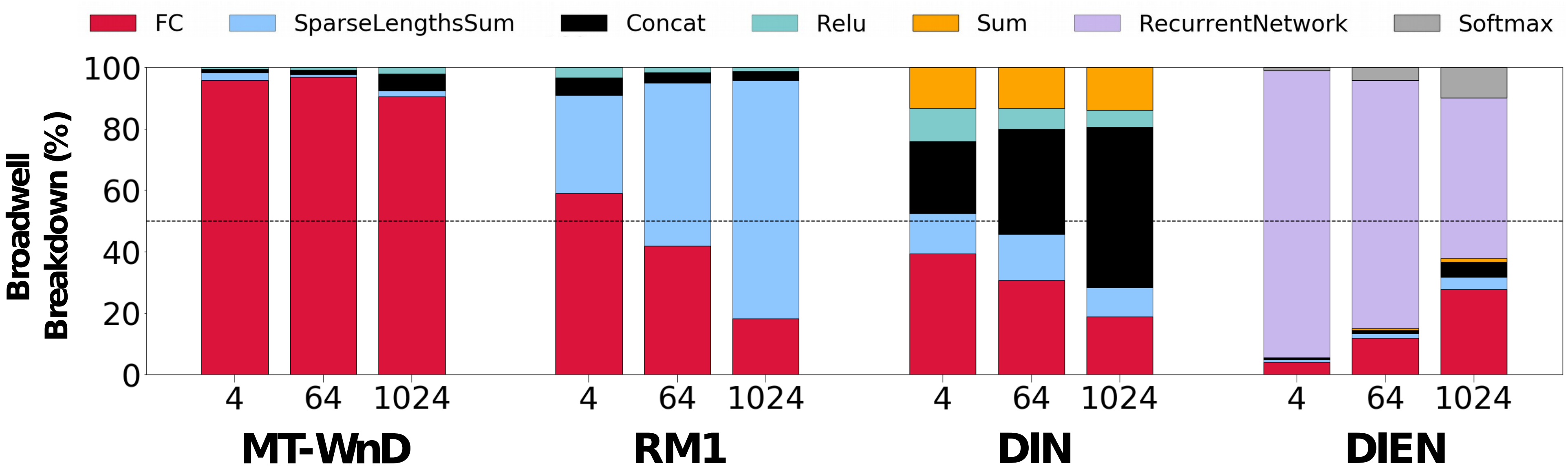


Can we explain the performance trends with **software level operators**?

Can we explain the performance trends with **microarchitectural analysis**?

Operator Breakdowns



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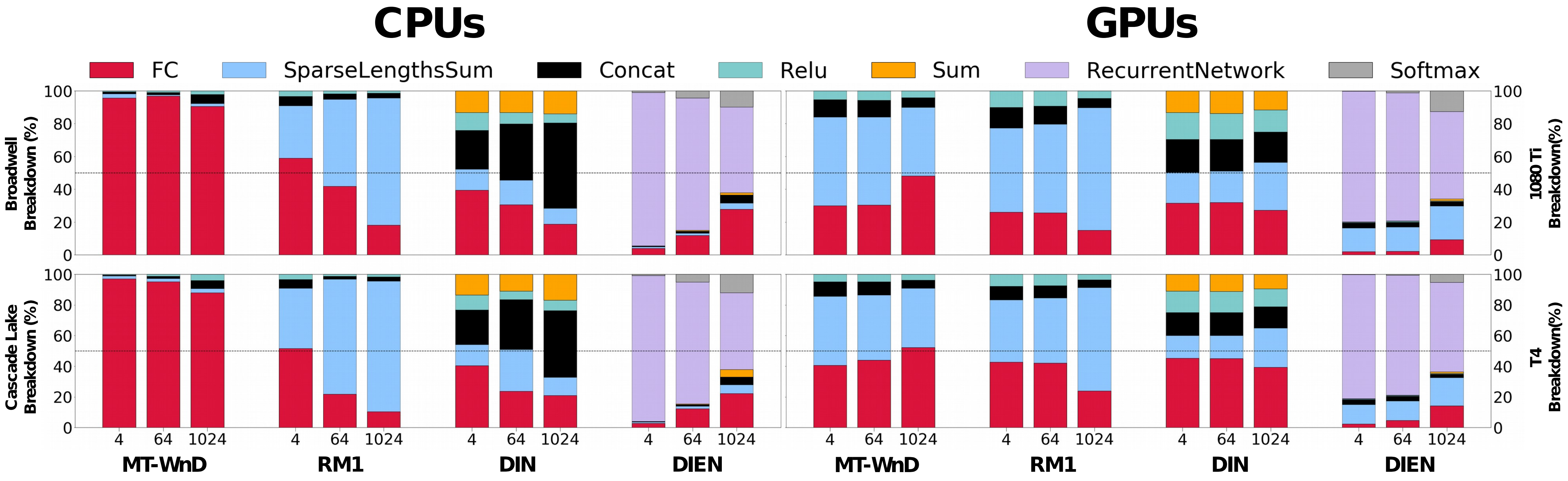

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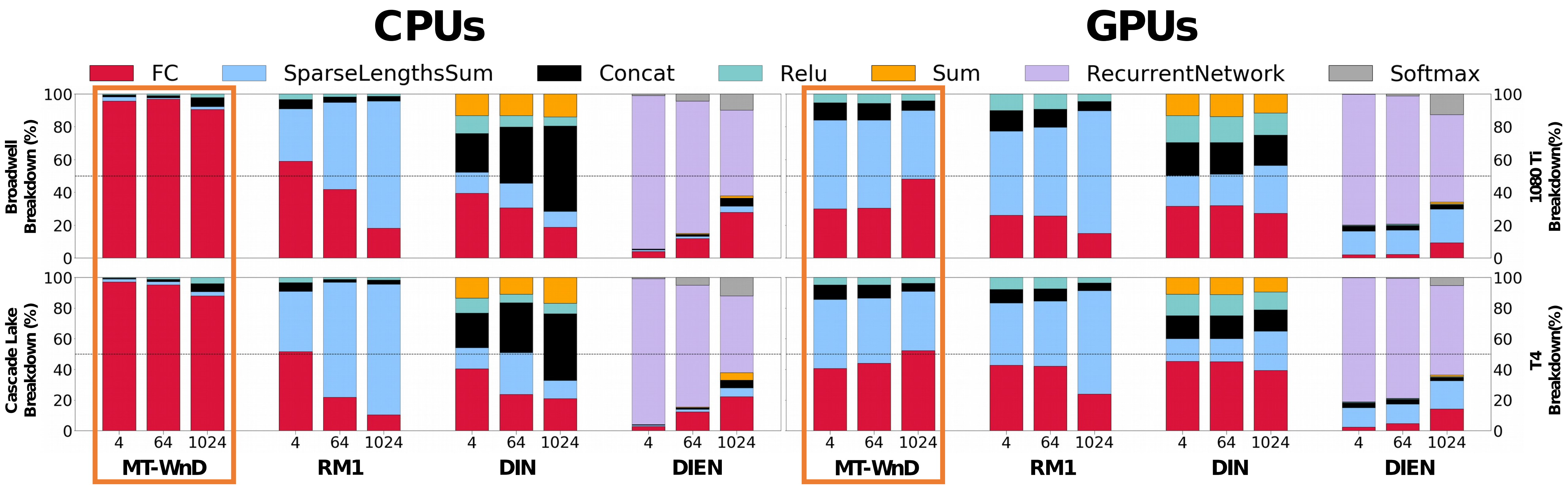
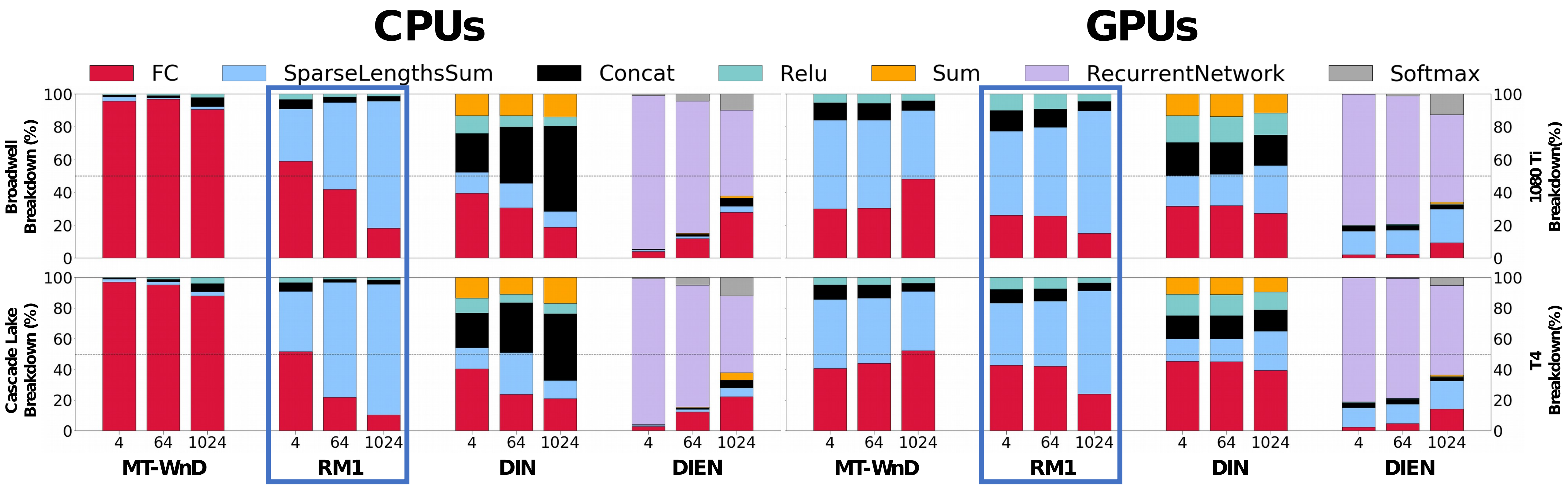


GPUs accelerate models dominated by **FC** operators on CPUs **by reducing the FC operator**

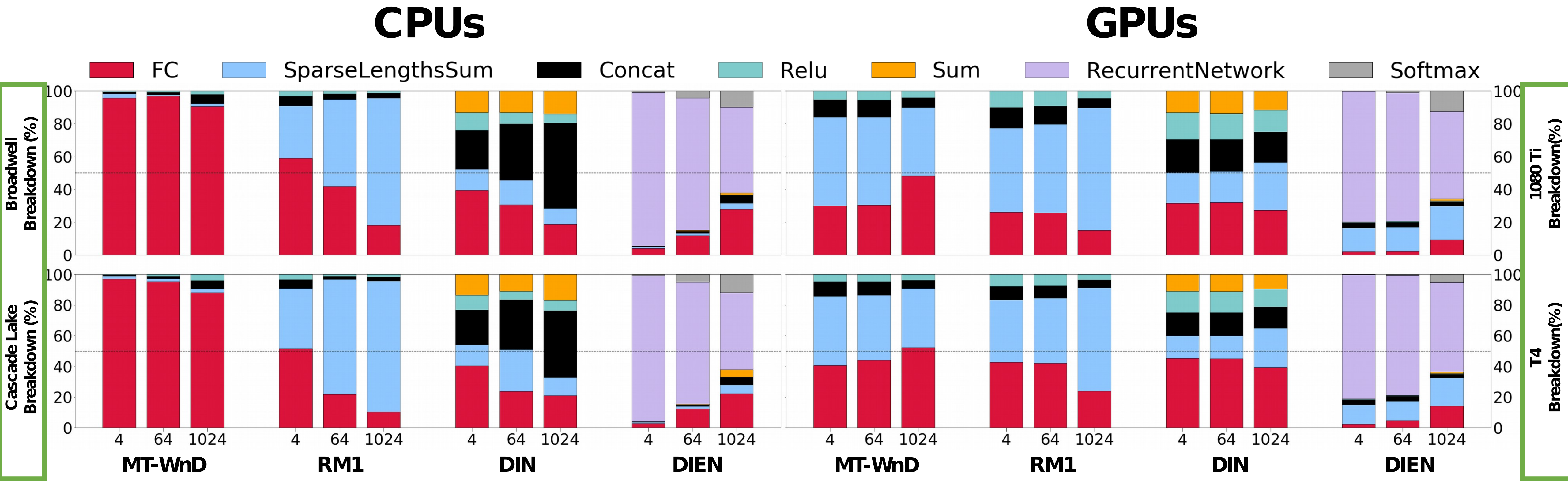
Operator Breakdowns



GPUs struggle with models dominated by **Embedding** operators on CPUs

due to data communication overheads

Operator Breakdowns

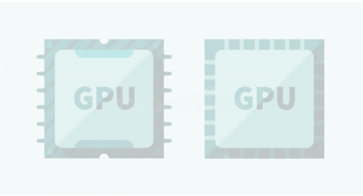


Different generations of the same platform type (i.e., CPU/GPU) **affect exact operator usages but retain general trends**.

Characterization

Question: What are the bottlenecks of each layer and how do they affect one another?

What do industry-representative algorithms (**model architectures**) look like?



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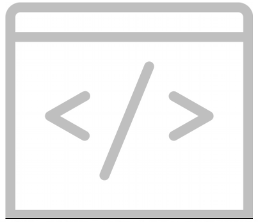
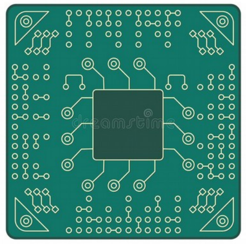
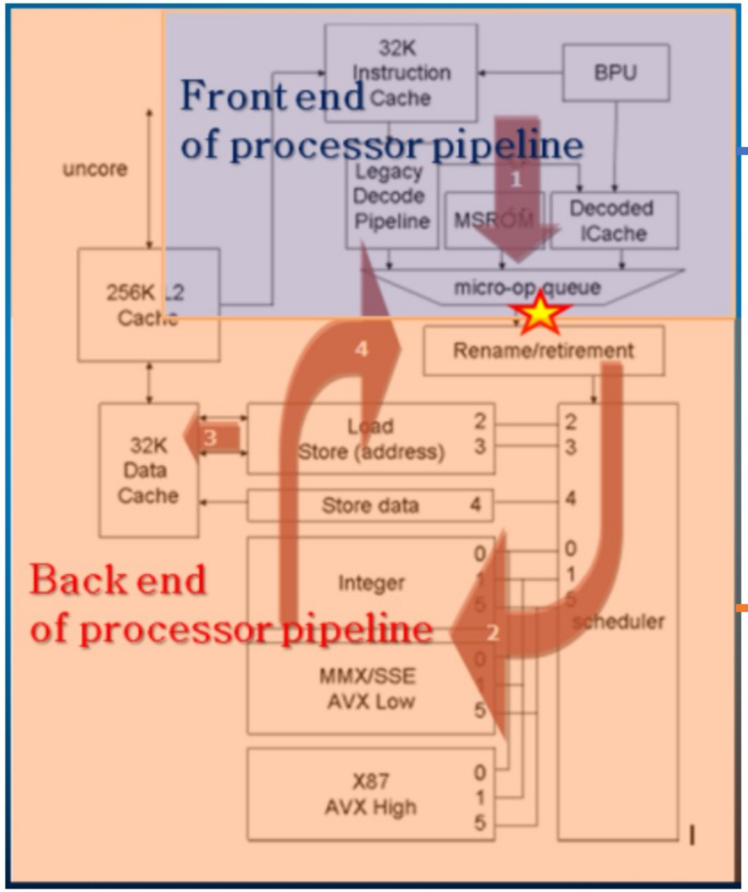


Can we explain the performance trends with **software level operators**?



Can we explain the performance trends with **microarchitectural analysis**?

TopDown Background



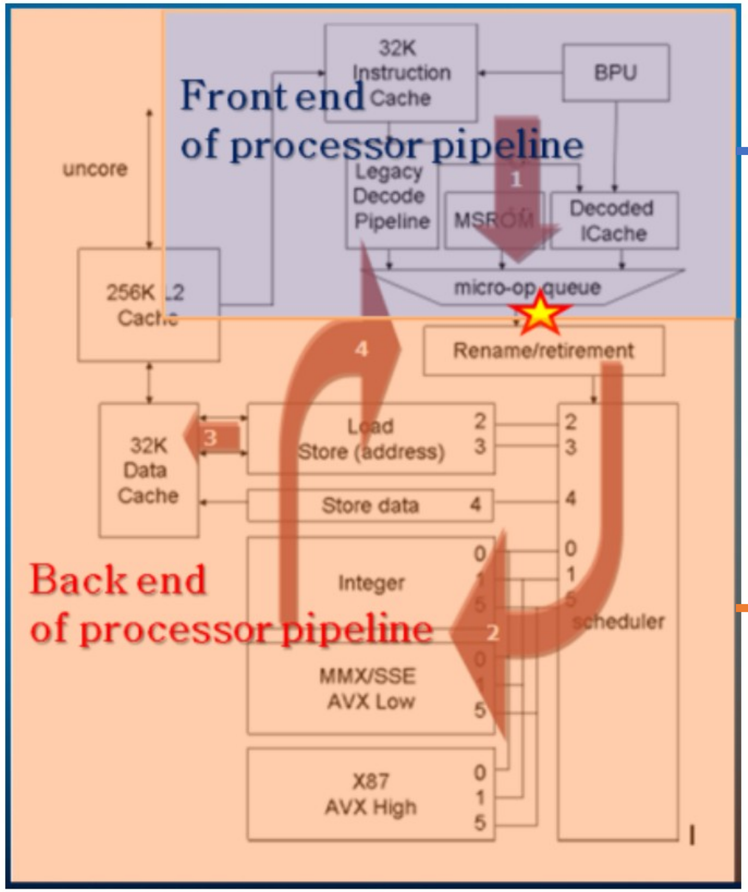
Latency Bound

Bandwidth Bound

Core Bound

Memory Bound

TopDown Background



Latency Bound

i-cache miss

Bandwidth Bound

instruction decoder inefficiency

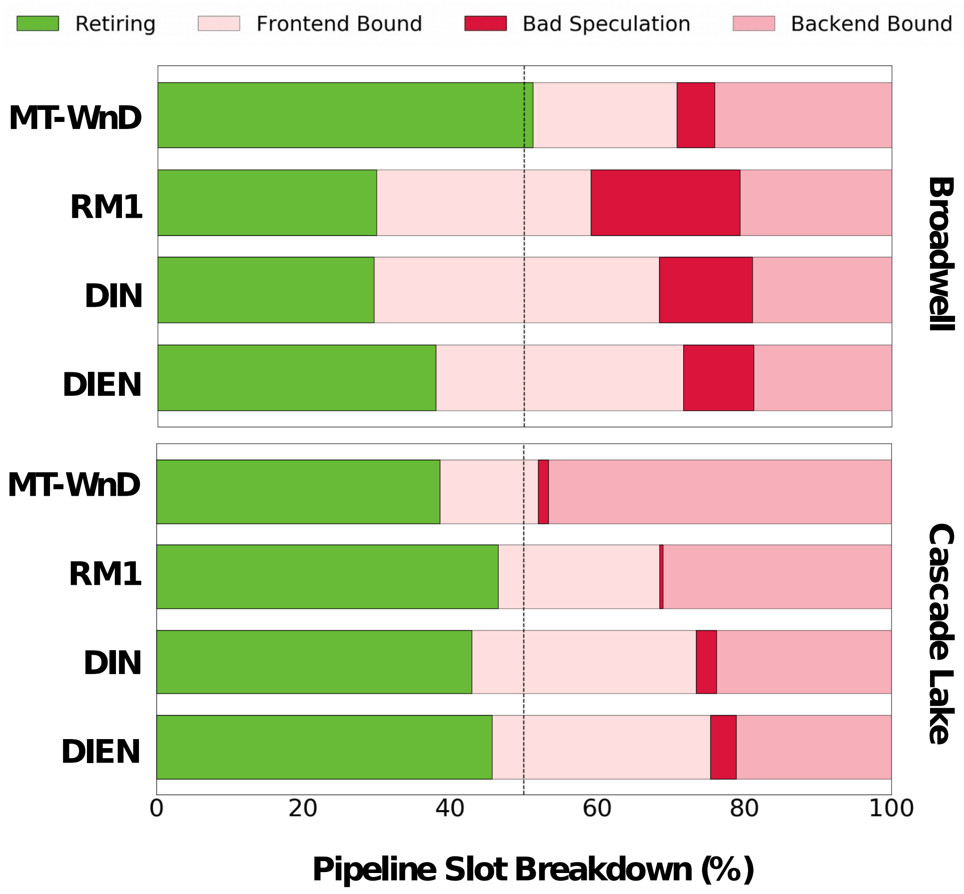
Core Bound

sub-optimal functional units

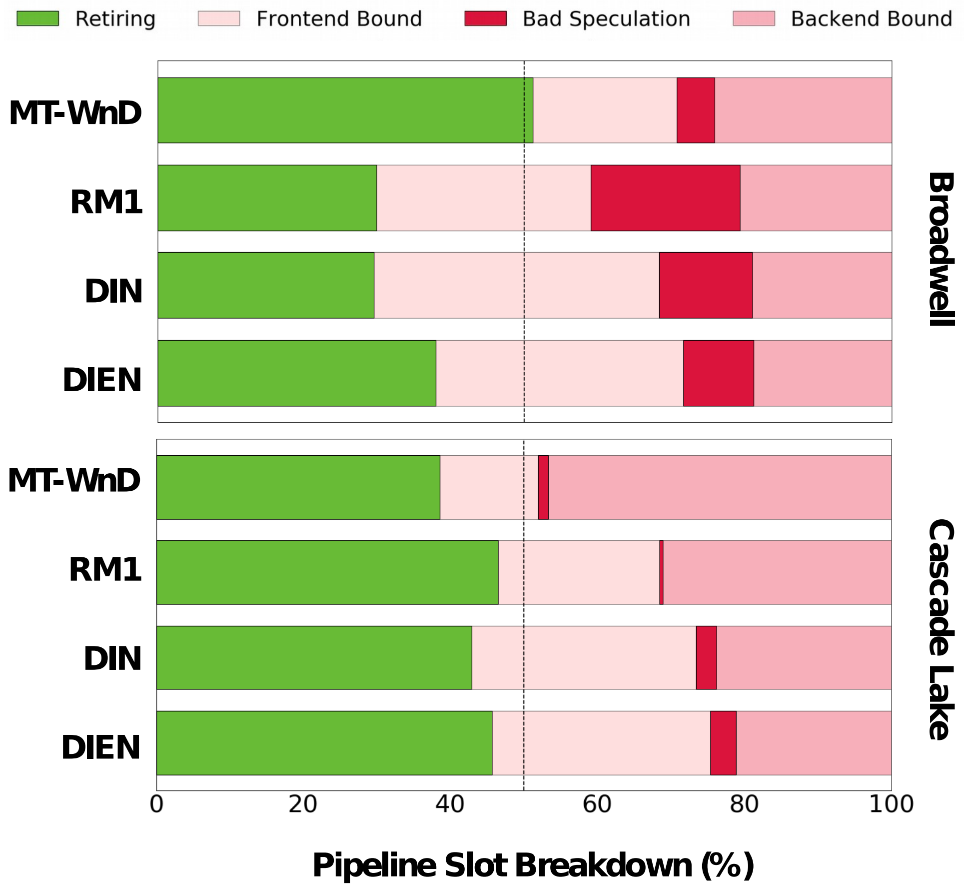
Memory Bound

d-cache miss/bandwidth

TopDown Pipeline Slot Breakdowns



On Broadwell, FC-dominated models **are limited by insufficient functional units**



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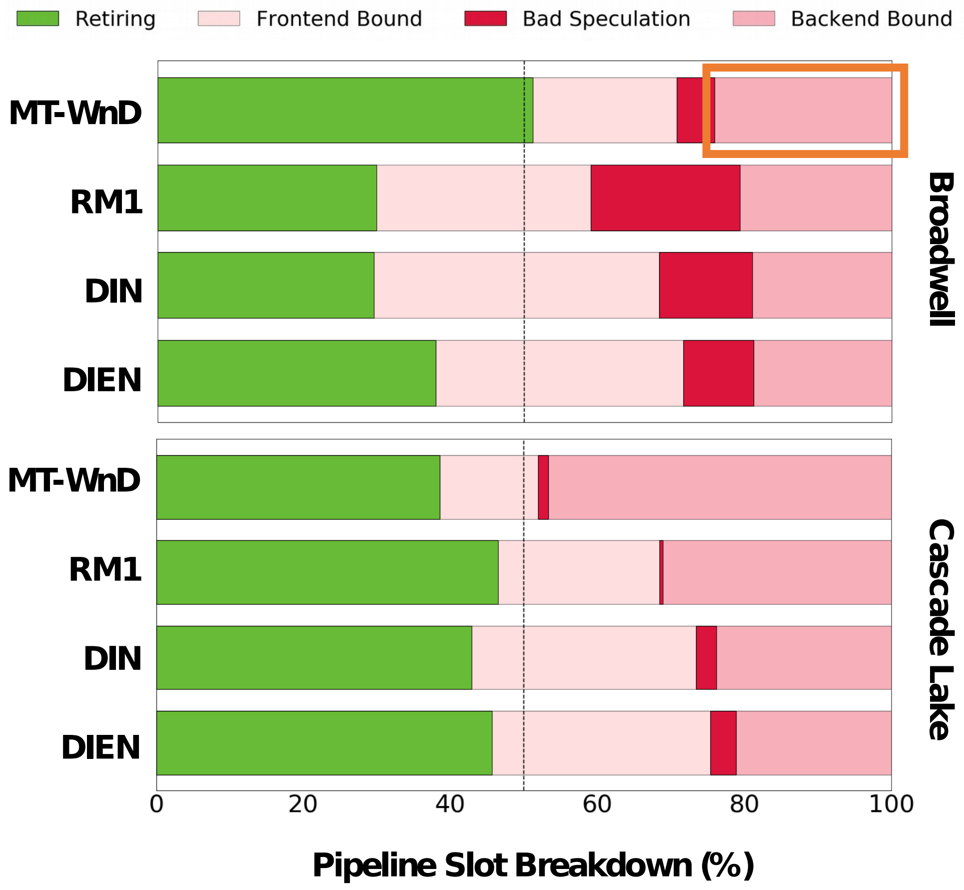

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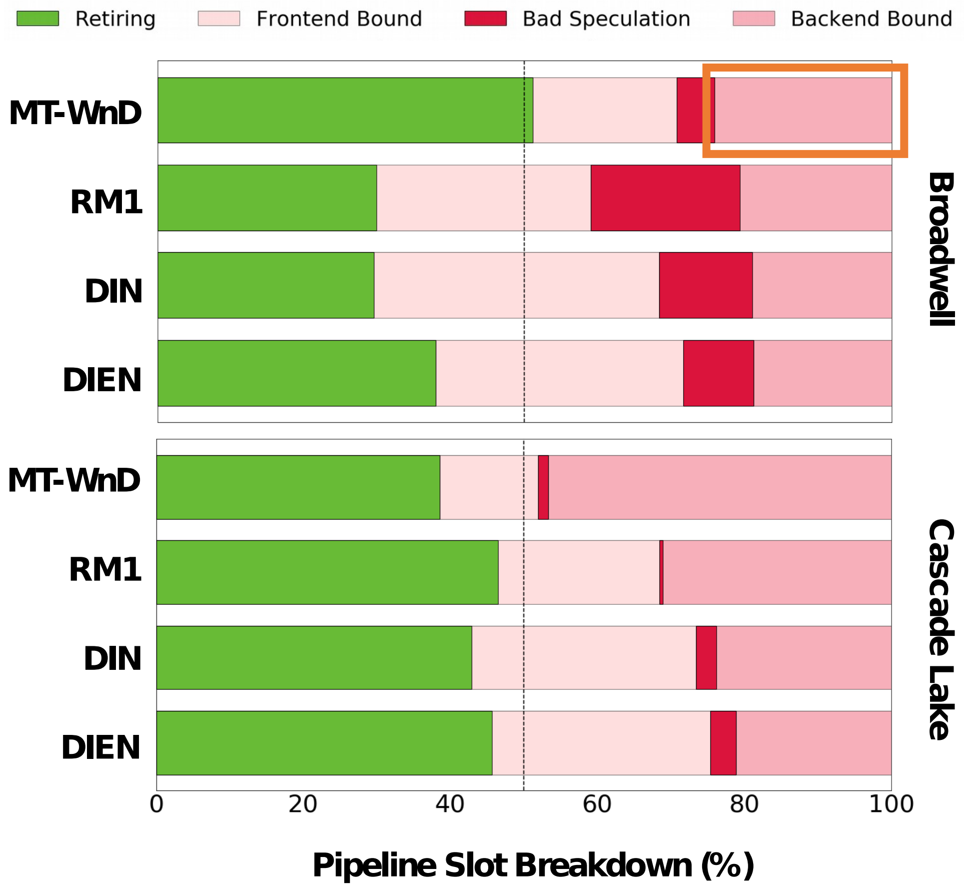

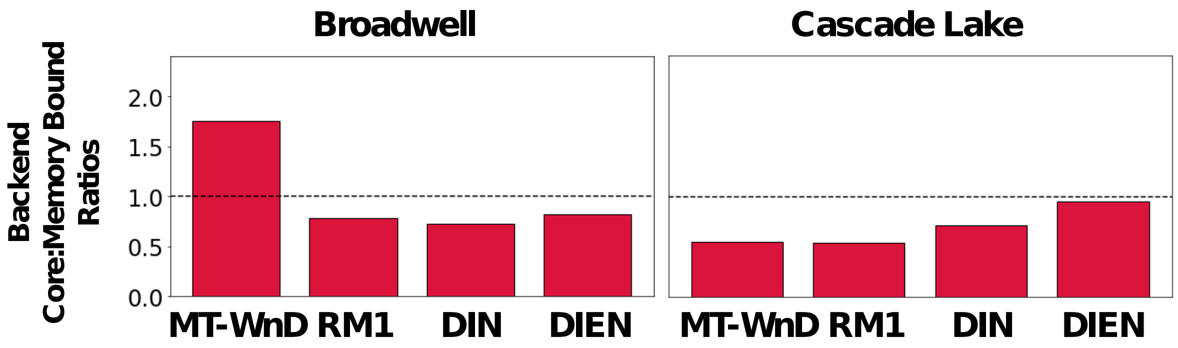

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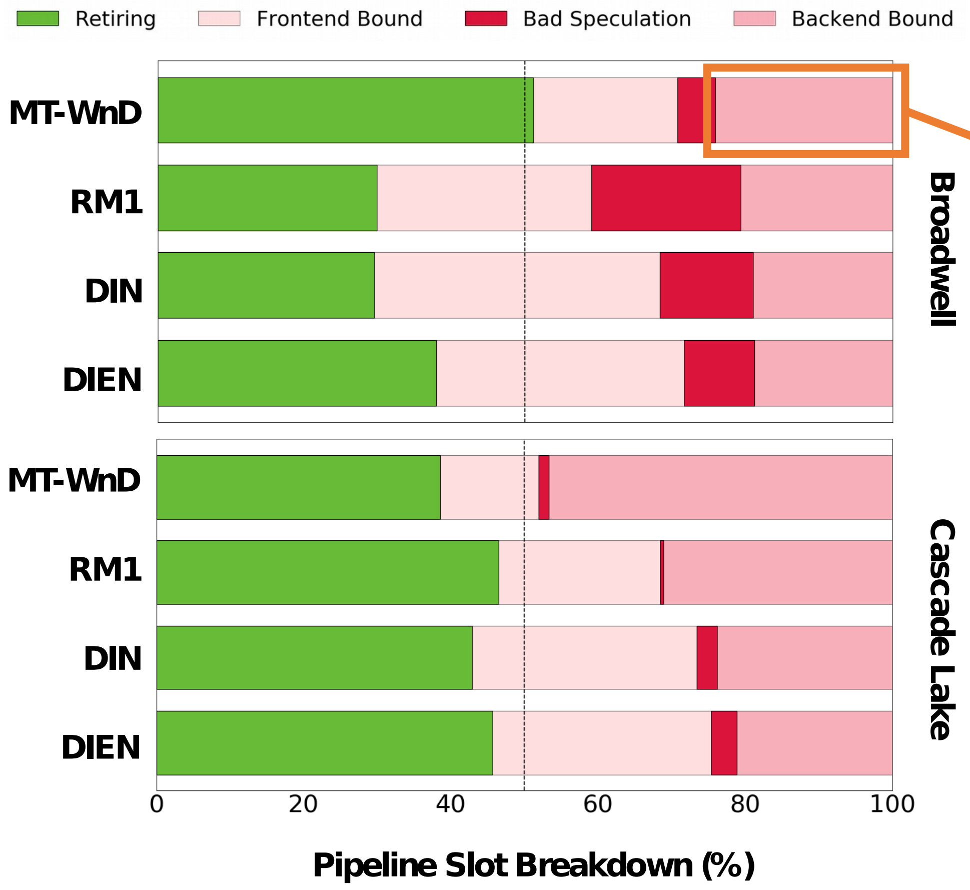
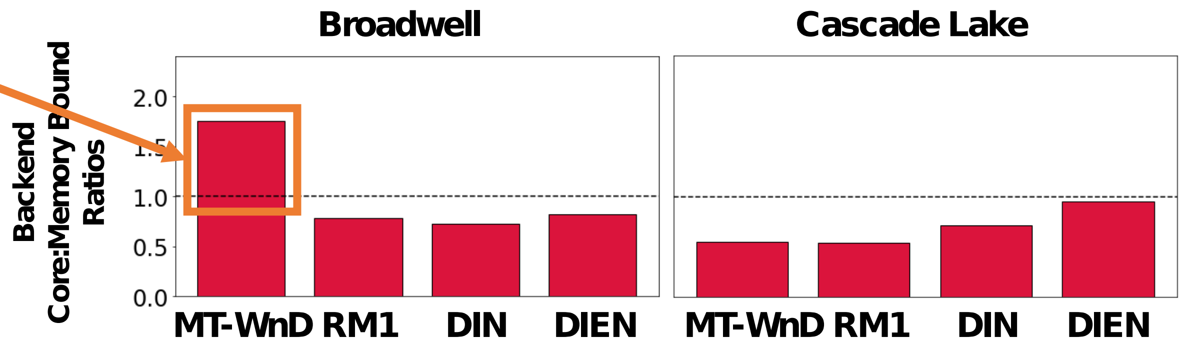
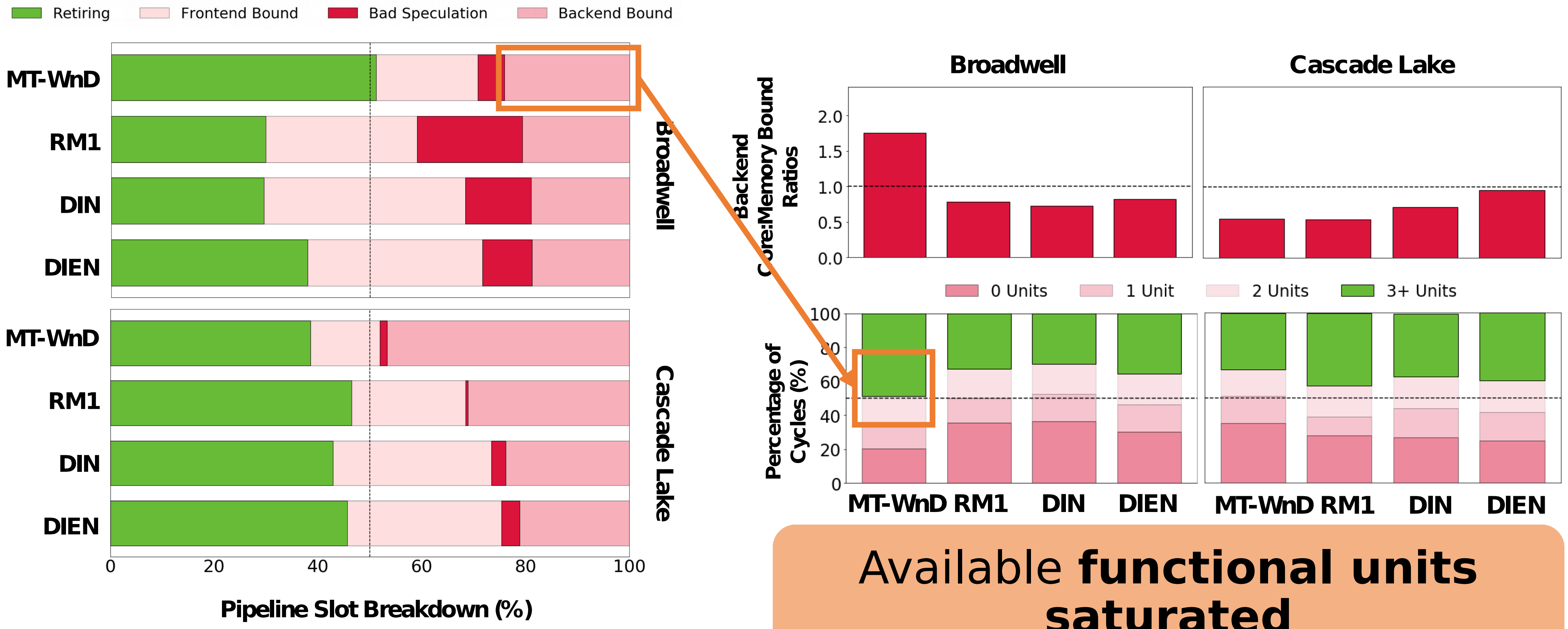




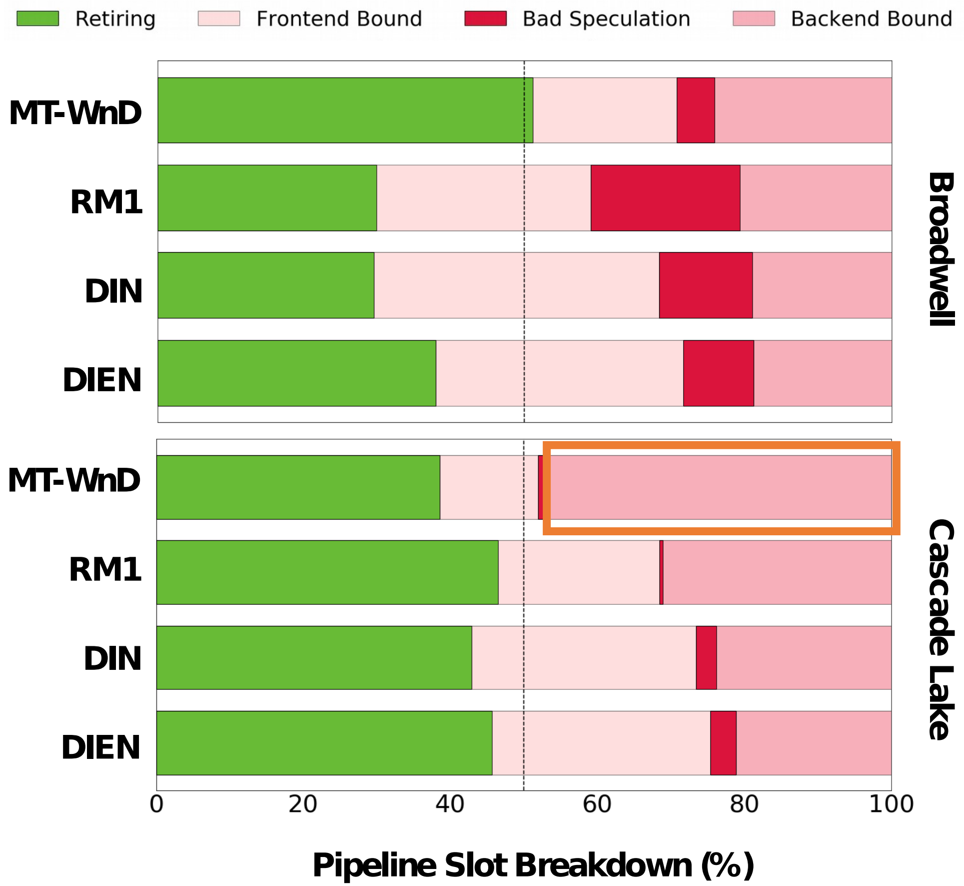
MT-WnD **core bound**!

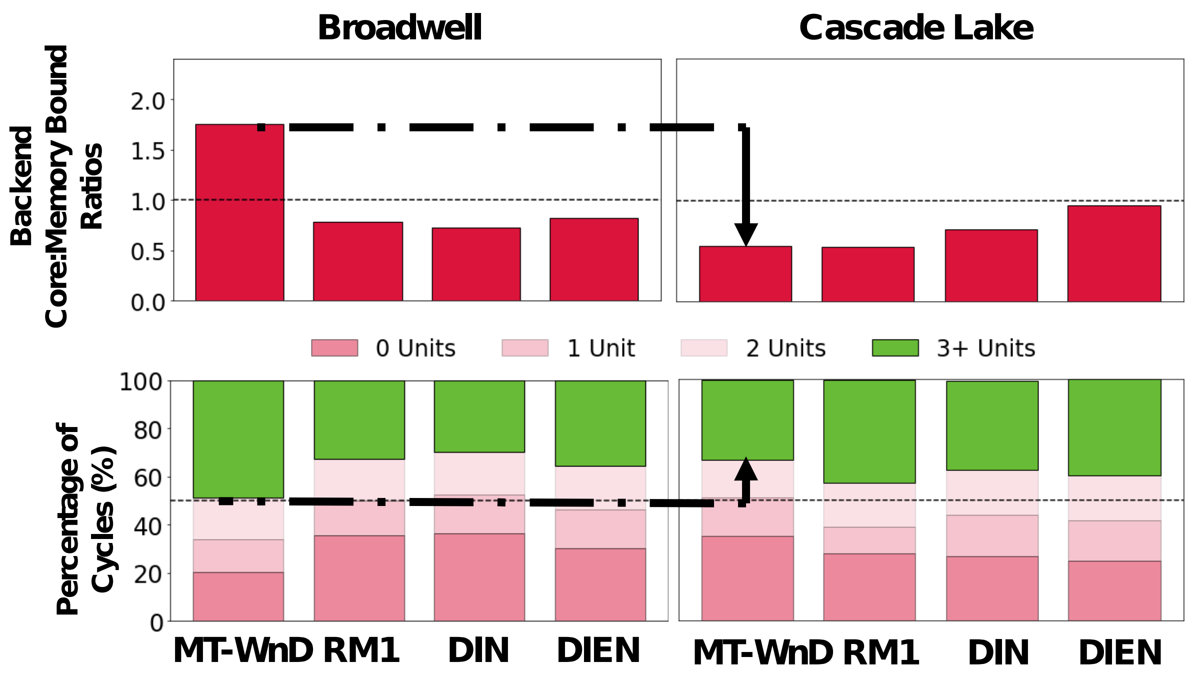
On Broadwell, FC-dominated models **are limited by insufficient functional units**



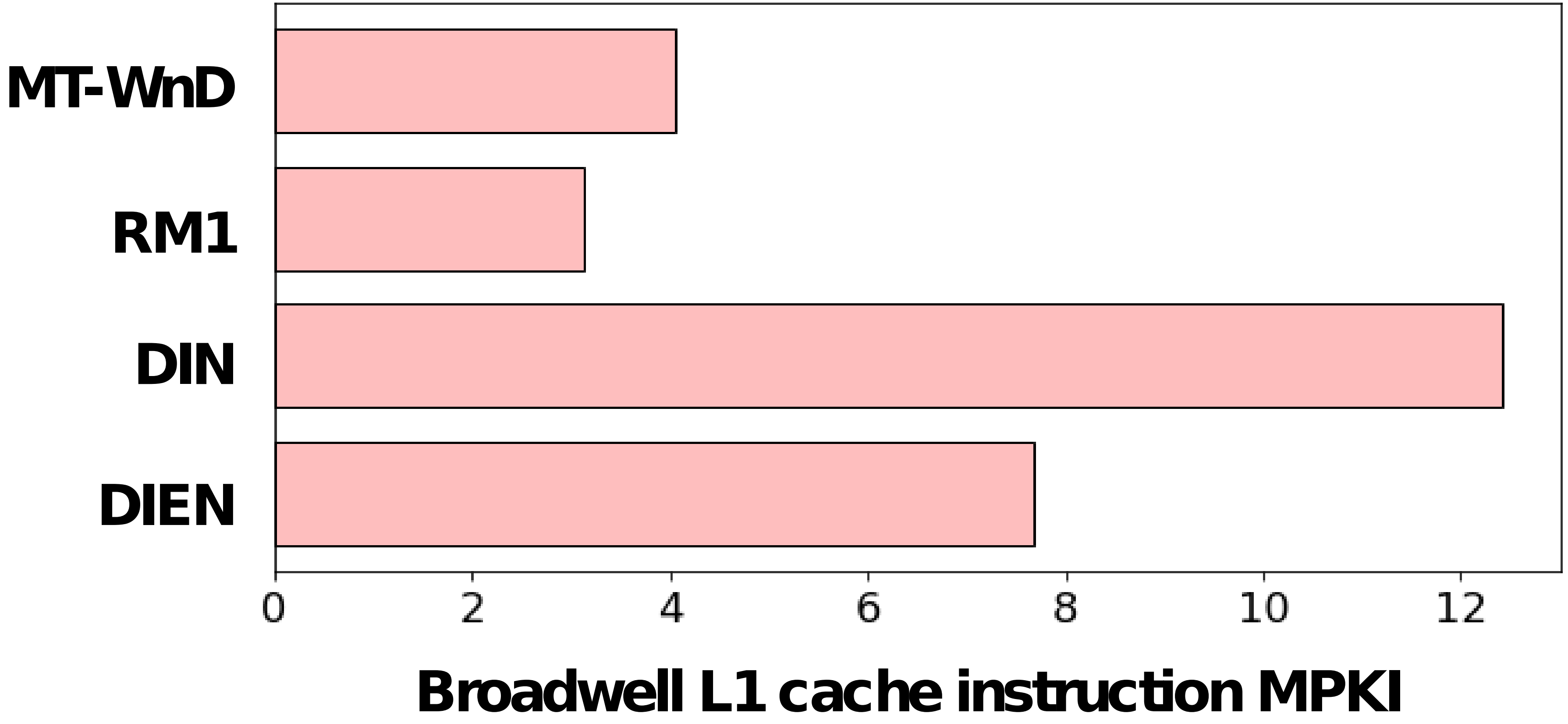
Available **functional units saturated**

On Cascade Lake, FC-dominated models **benefit from wider SIMD**, **shifting bottlenecks to memory subsystem**



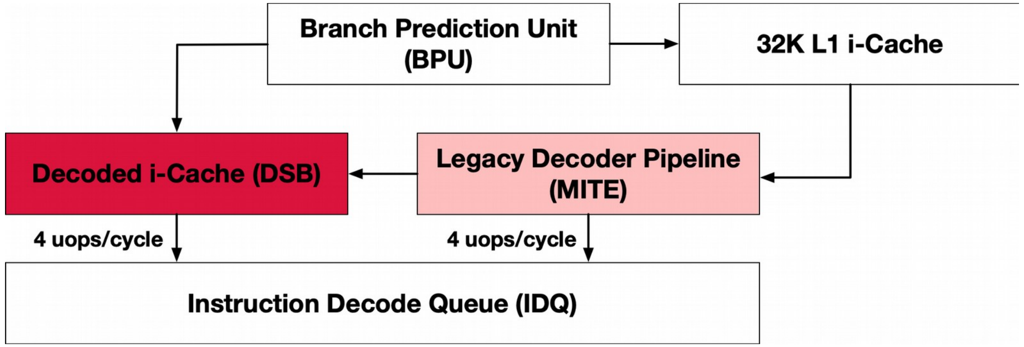


Attention-based models suffer from frontend latency (**L1 instruction-cache misses)**



Models with more embedding table lookups suffer from **instruction decoder bottlenecks**

Broadwell Frontend Decoder Pipeline



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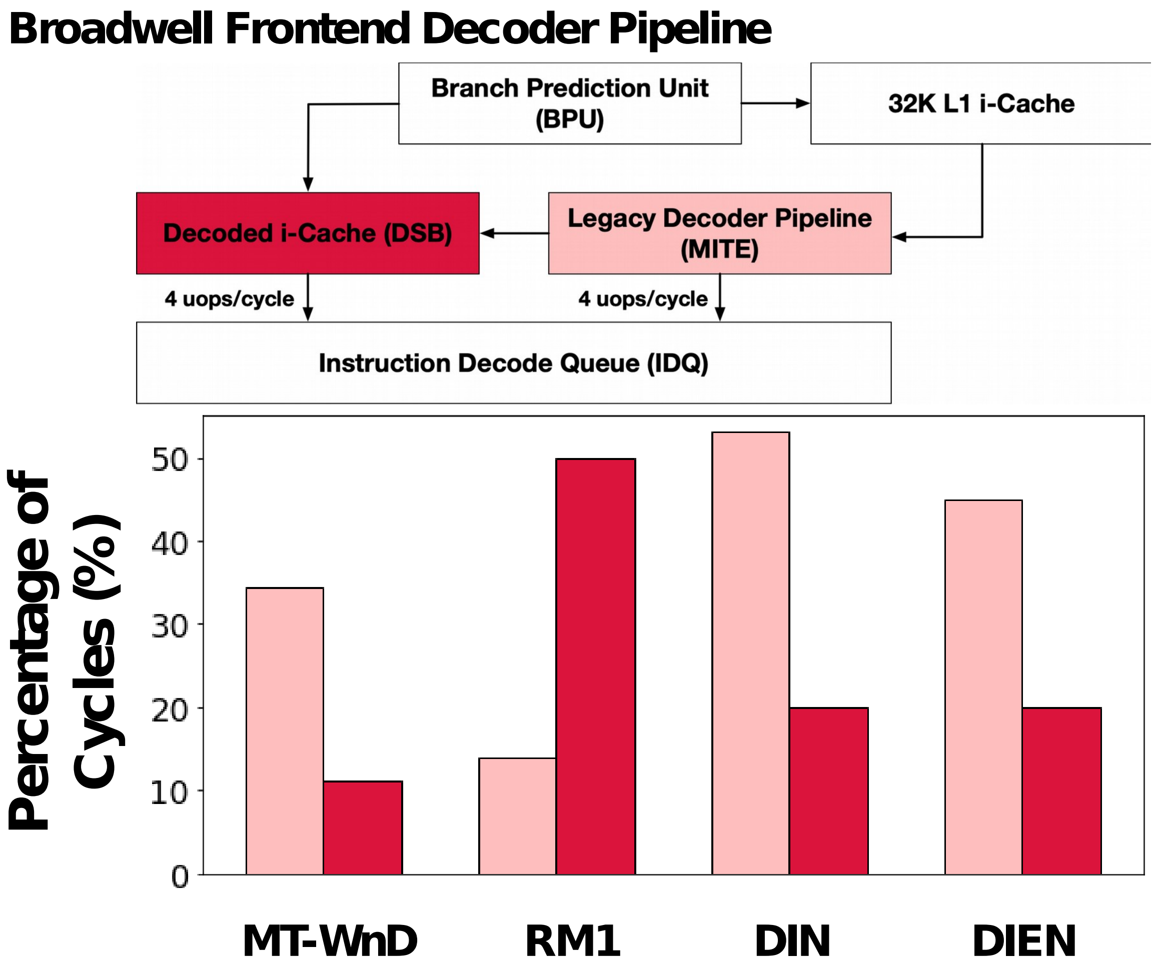

CPU Cycles limited due to Frontend Decoder Pipeline

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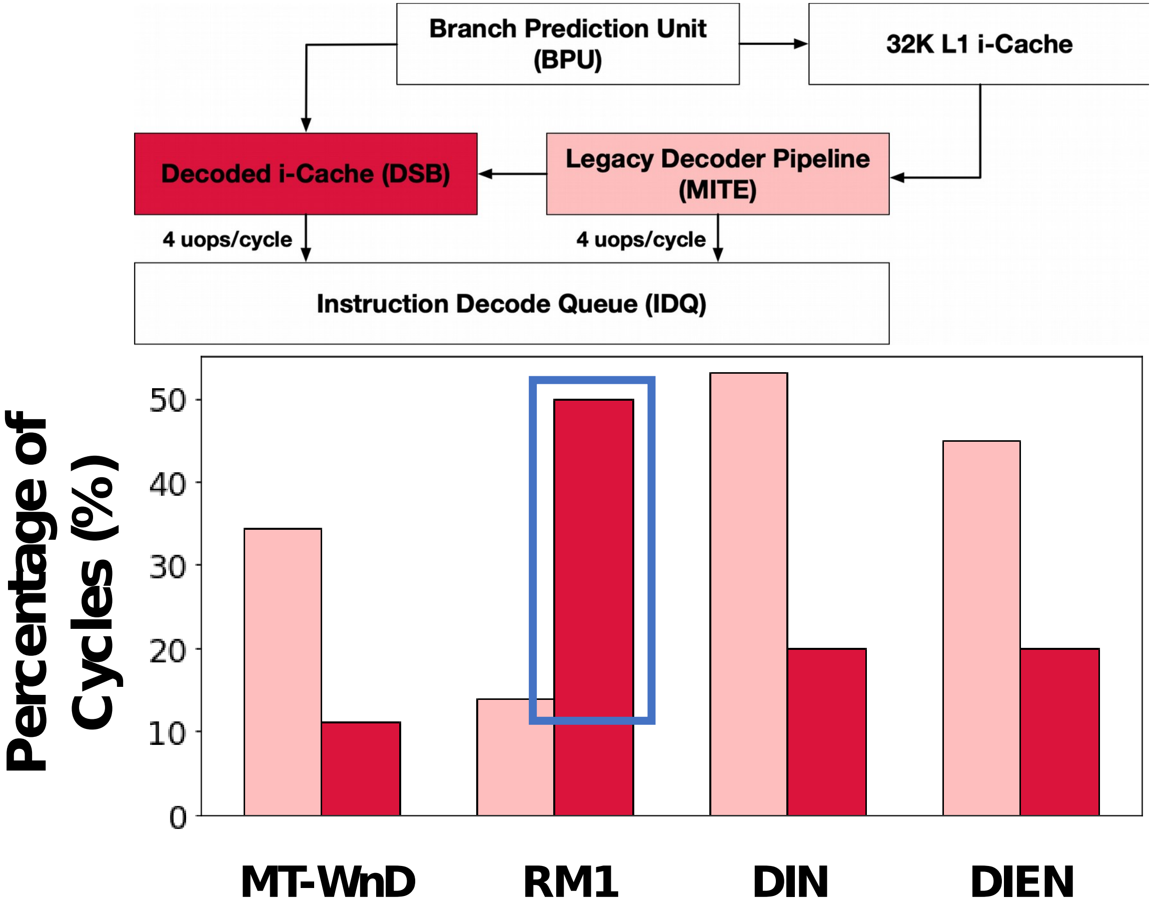
Broadwell Frontend Decoder Pipeline



DSB ineffective for RM1!

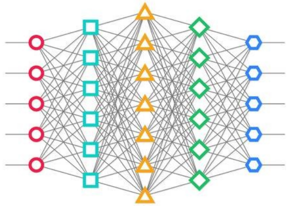
CPU Cycles limited due to Frontend Decoder Pipeline

Summary of Microarchitectural Effects

Type of Model	Microarchitectural Insight
FC Heavy	On Broadwell, **insufficient functional units** On Cascade Lake, **sub-optimal memory subsystem**
Attention Heavy	Frontend Latency L1 i-cache miss rate (**L1 i-MPKI**)
Embedding Heavy	Frontend Bandwidth Decoded i-cache (**DSB**)

Characterization

Question: What are the bottlenecks of each layer and how do they affect one another?



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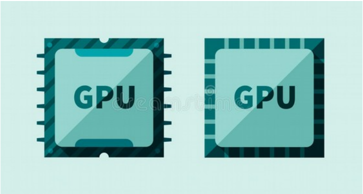

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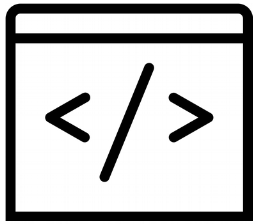

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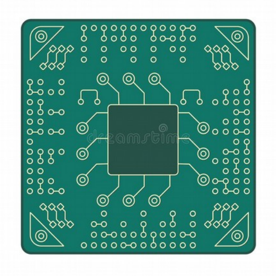


Can we explain the performance trends with **<u>microarchitectural analysis</u>**?

Characterization

2020 IEEE International Symposium on Workload Characterization (IISWC)

Cross-Stack Workload Characterization of Deep Recommendation Systems

Samuel Hsia[1], Udit Gupta[1,2], Mark Wilkening[1],
Carole-Jean Wu[2], Gu-Yeon Wei[1], David Brooks[1]

More algorithms

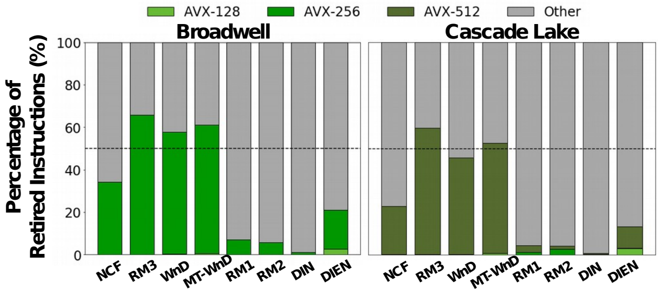
More characterization

Open-Source

Google Play

NETFLIX

More industry-representative deep recommendation models



More microarchitectural insights based on detailed PMU counter analysis

Model implementations and experiment scripts open-sourced: https://github.com/harvard-acc/DeepRecSys

This talk

Characterization

[IISWC '20]

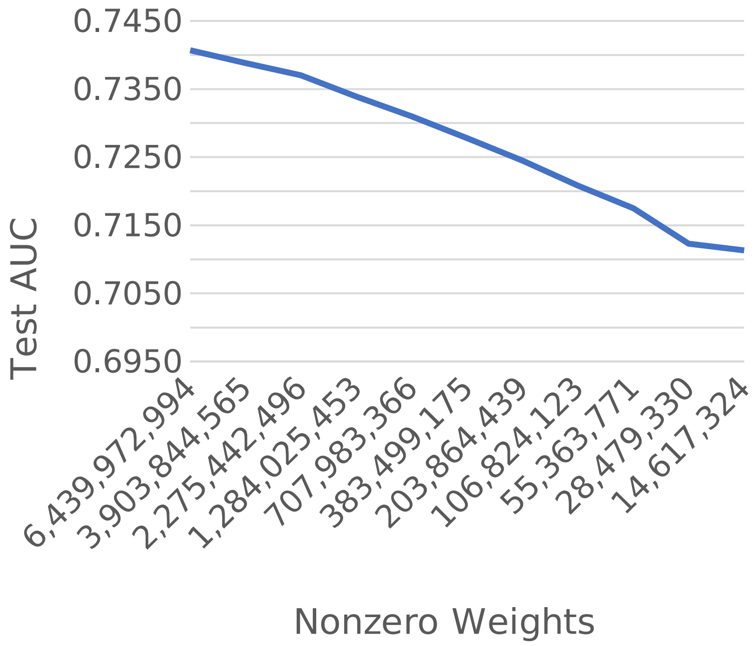
RecSSD

[ASPLOS '21]

Computational Trends in Recommendation

Computational Trends in Recommendation

More Features, More Accuracy



[1]

ing Massive Scale Deep Learning Ads Systems with GPUs and SSDs”, PeRSonAl at ISCA 2020, Weijie Zhao

Computational Trends in Recommendation

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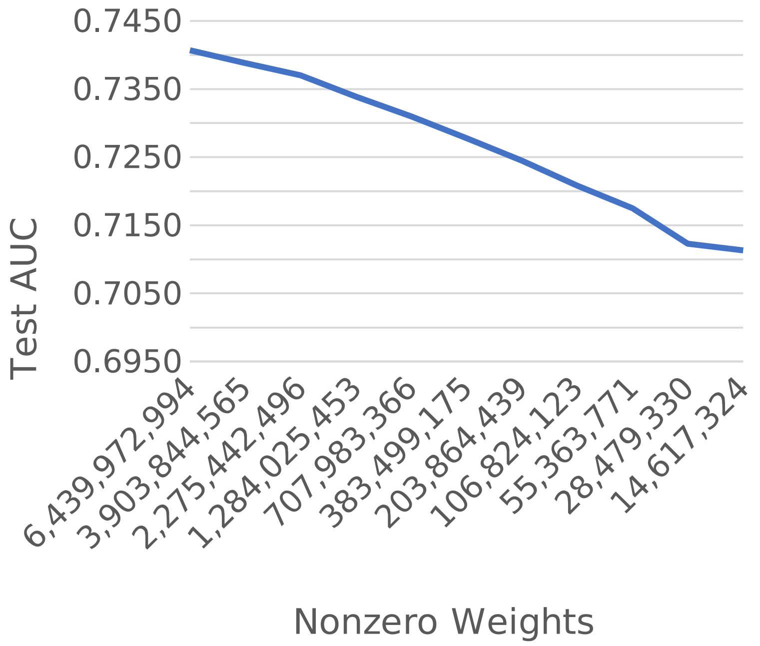
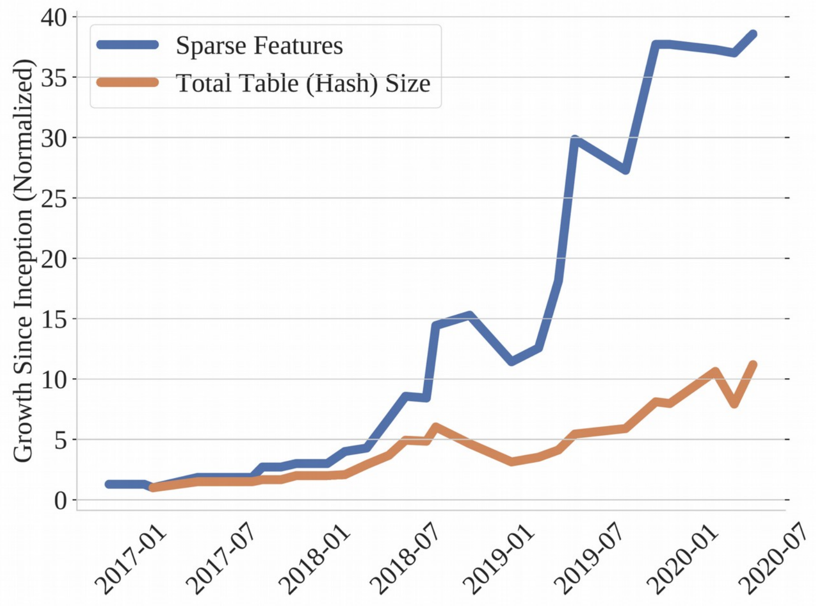


[1]

… And Memory Capacity



[2]

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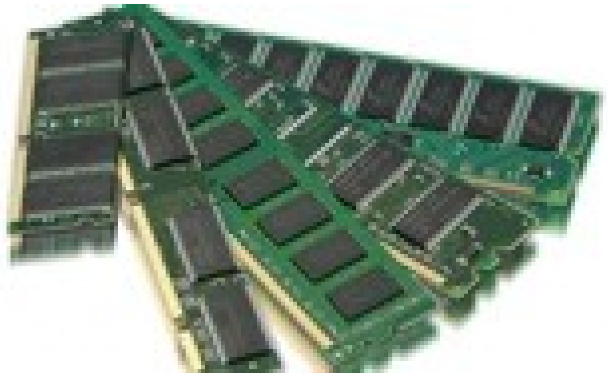
erstanding Capacity-Driven Scale-Out Neural Recommendation Inference", arXiv:2011.02084, Lui et. al.

High-Capacity Flash vs. DRAM



High-Capacity Flash vs. DRAM

Cost

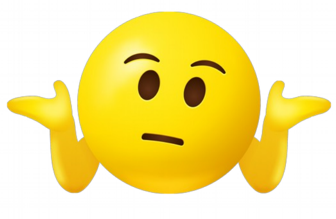
O(5-10X)

O(X)

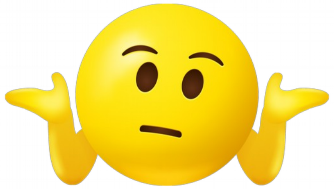
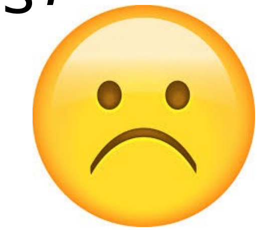
High-Capacity Flash vs. DRAM

	Cost	Read Latency
	O(5-10X)	O(10ns)
	O(X)	O(10us)
		

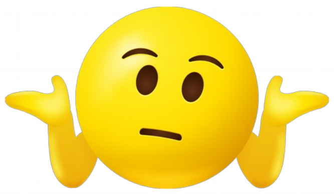
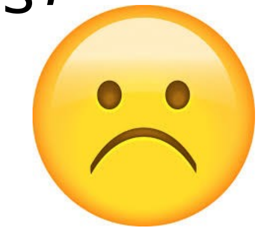
High-Capacity Flash vs. DRAM

	Cost	Read Latency	Write Latency
	O(5-10X)	O(10ns)	O(10ns)
	O(X)	O(10us)	O(1ms)
			

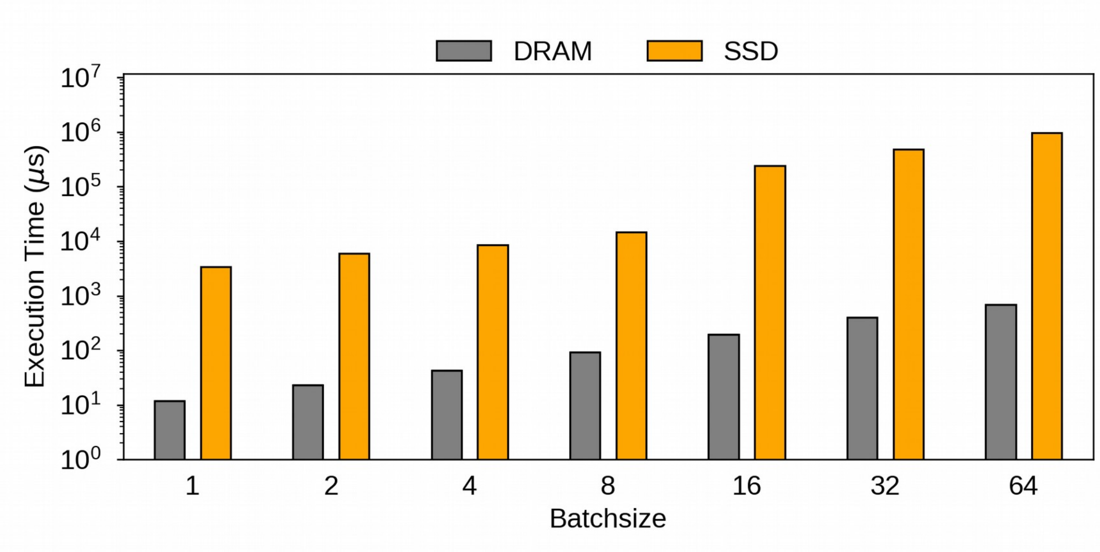
High-Capacity Flash vs. DRAM

	Cost	Read Latency	Write Latency	Random 4KB Read B/W
	O(5-10X)	O(10ns)	O(10ns)	O(75GB/s)
	O(X)	O(10us)	O(1ms)	O(2-3GB/s)
				

High-Capacity Flash vs. DRAM

	Cost	Read Latency	Write Latency	Random 4KB Read B/W	Random 128B
	O(5-10X)	O(10ns)	O(10ns)	O(75GB/s)	O(75GB/s)
	O(X)	O(10us)	O(1ms)	O(2-3GB/s)	O(10MB/s)
					

Flash SSDs for Recommendation



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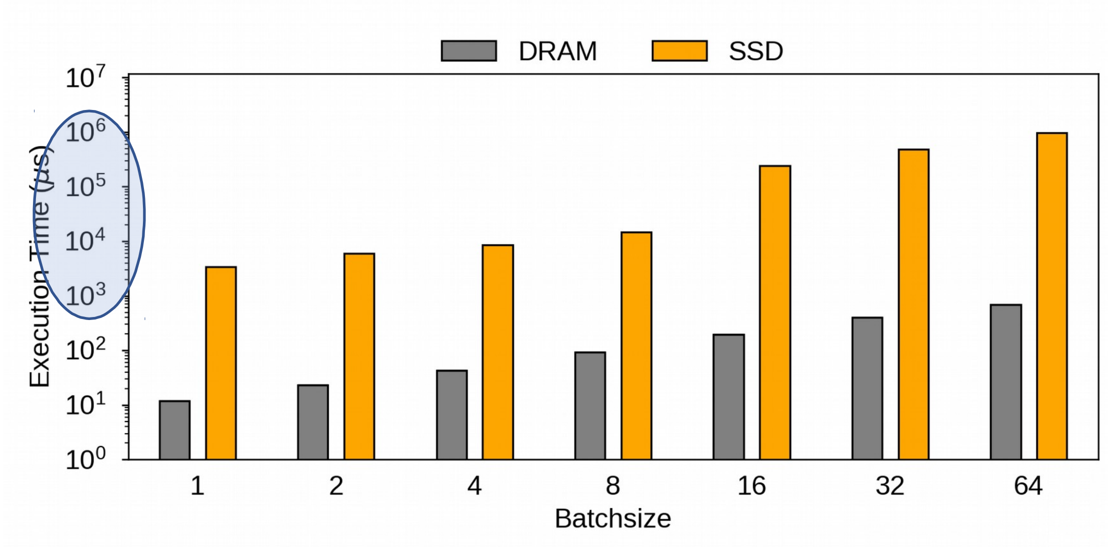


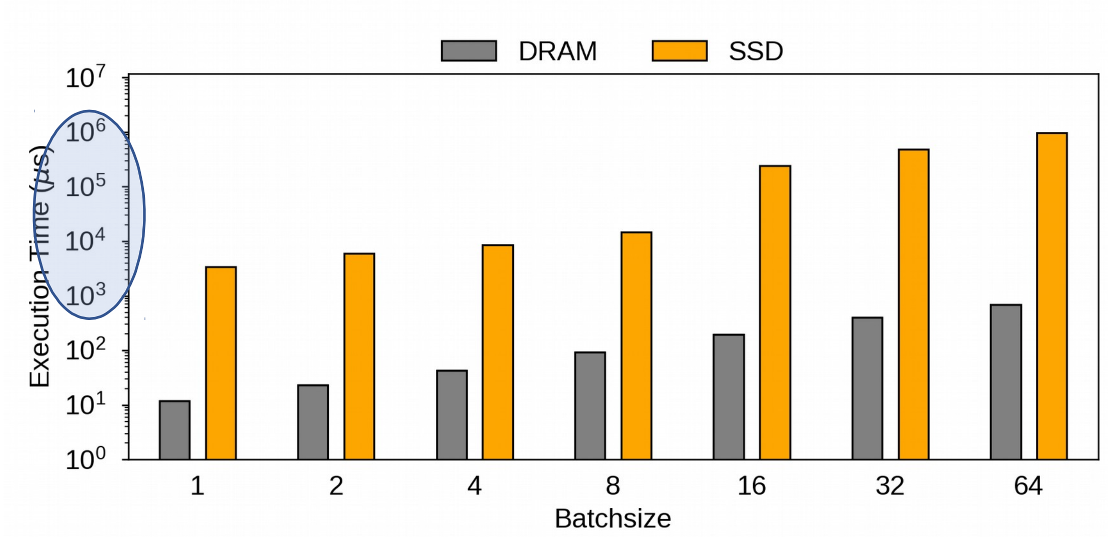
3 Orders of magnitude slower embedding operations

Low Bandwidth

Page Size vs. Access Size

Software Overheads in PCIe Access

Flash SSDs for Recommendation



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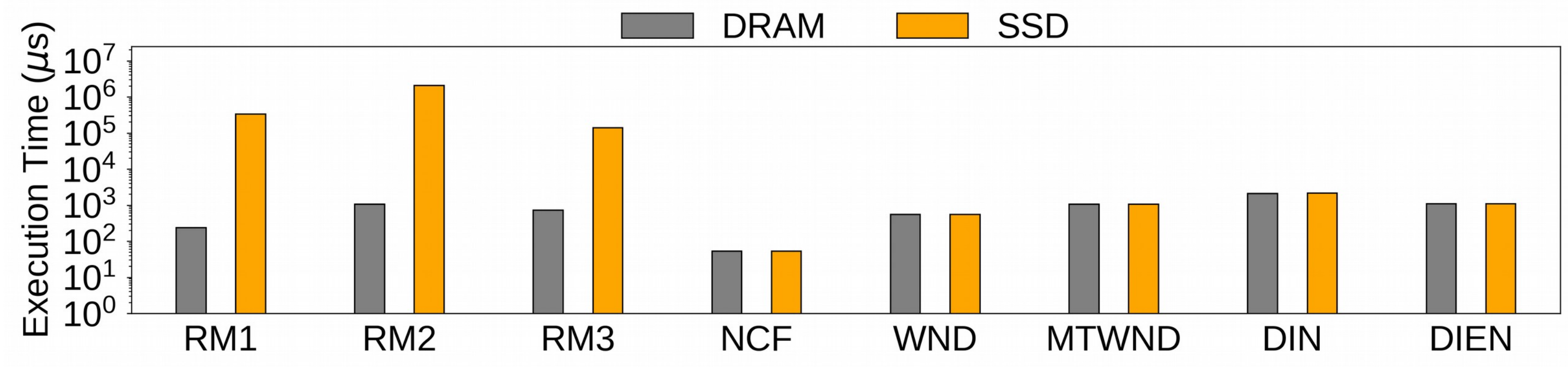

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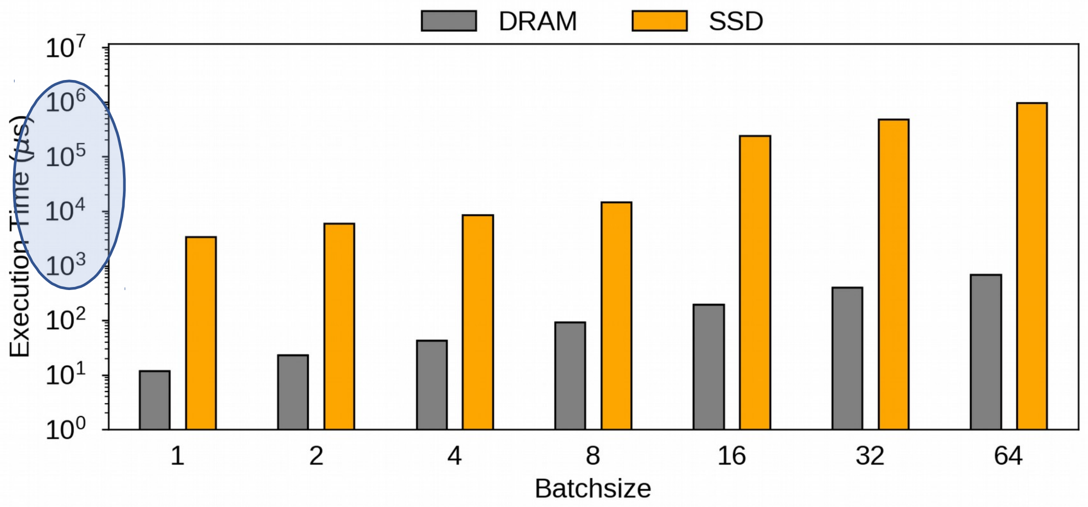

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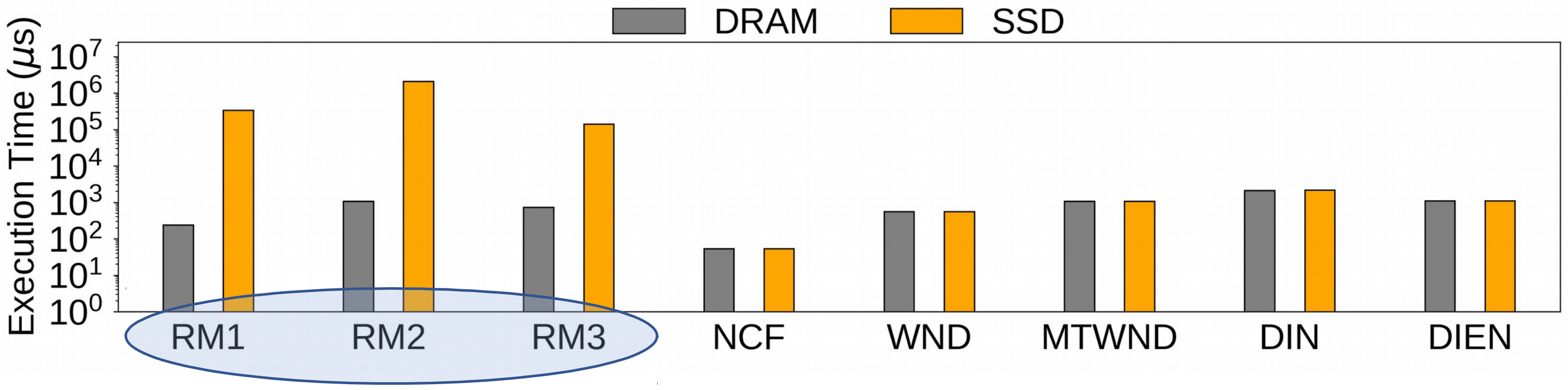

Significant slowdown in embedding dominated models

Problems with Flash for Recommendation

Low Bandwidth

Page and Access Size Mismatch

Software Overheads in PCIe Access

Problems with Flash for Recommendation

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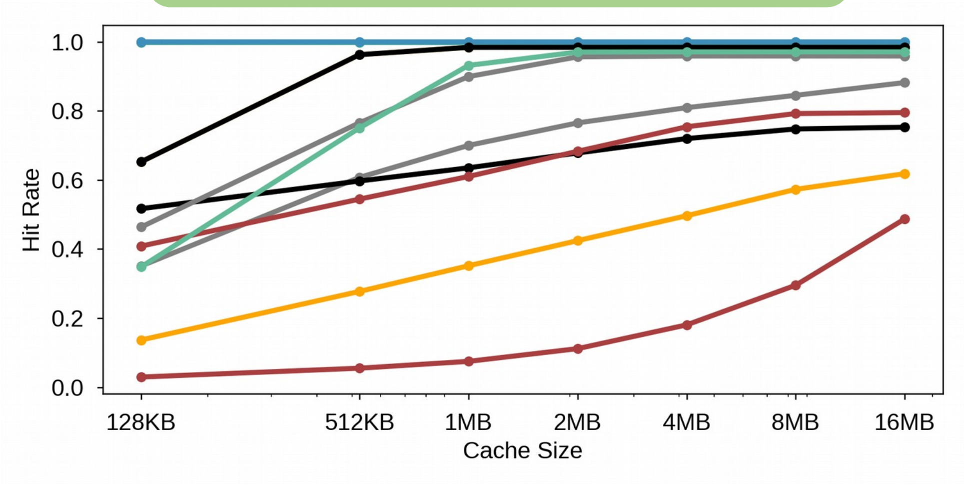
Software Overheads in PCIe Access

DRAM Caching



Hit-rates vary wildly across embedding tables from 10% to 90%

Problems with Flash for Recommendation

Low Bandwidth

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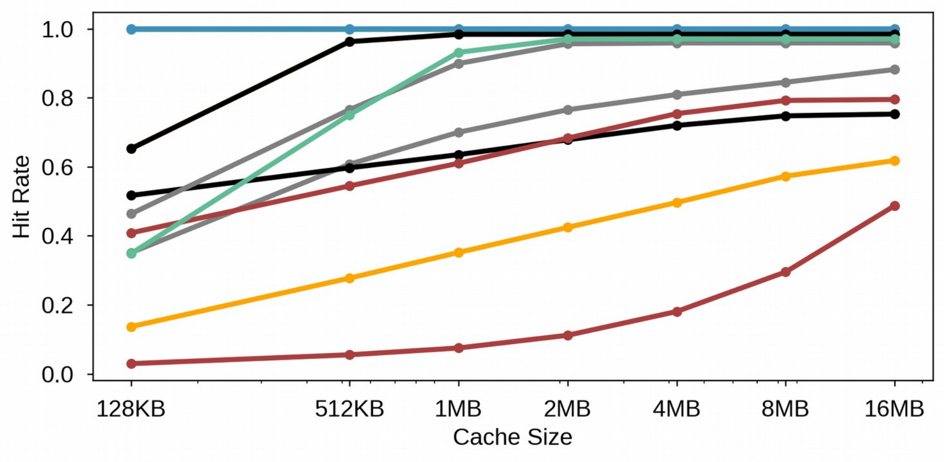

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Page and Access Size Mismatch

Table re-ordering, advanced caching

Bandana [1]

Smaller flash page sizes in SSD hardware, byte addressable NVM

Software Overheads in PCIe Access

[1] "Bandana: Using Non-volatile Memory for Storing Deep Learning Models", SysML 19, Eisenman et. al.

Problems with Flash for Recommendation

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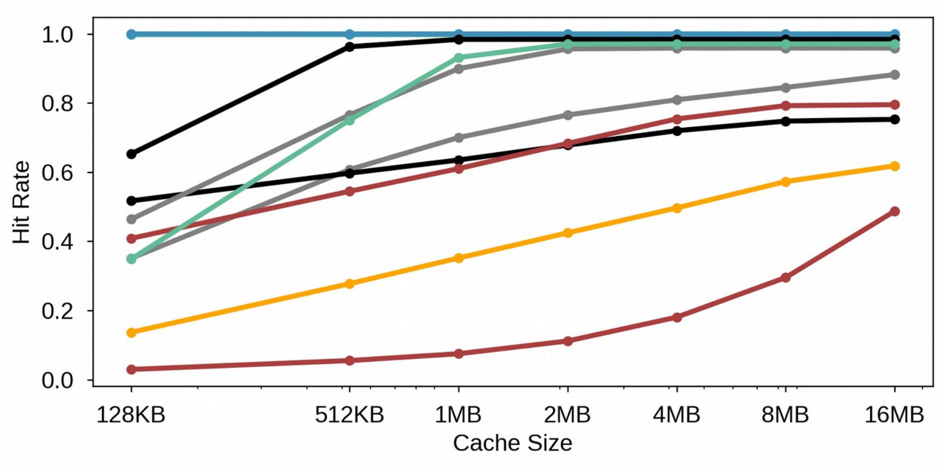

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Near Data Processing

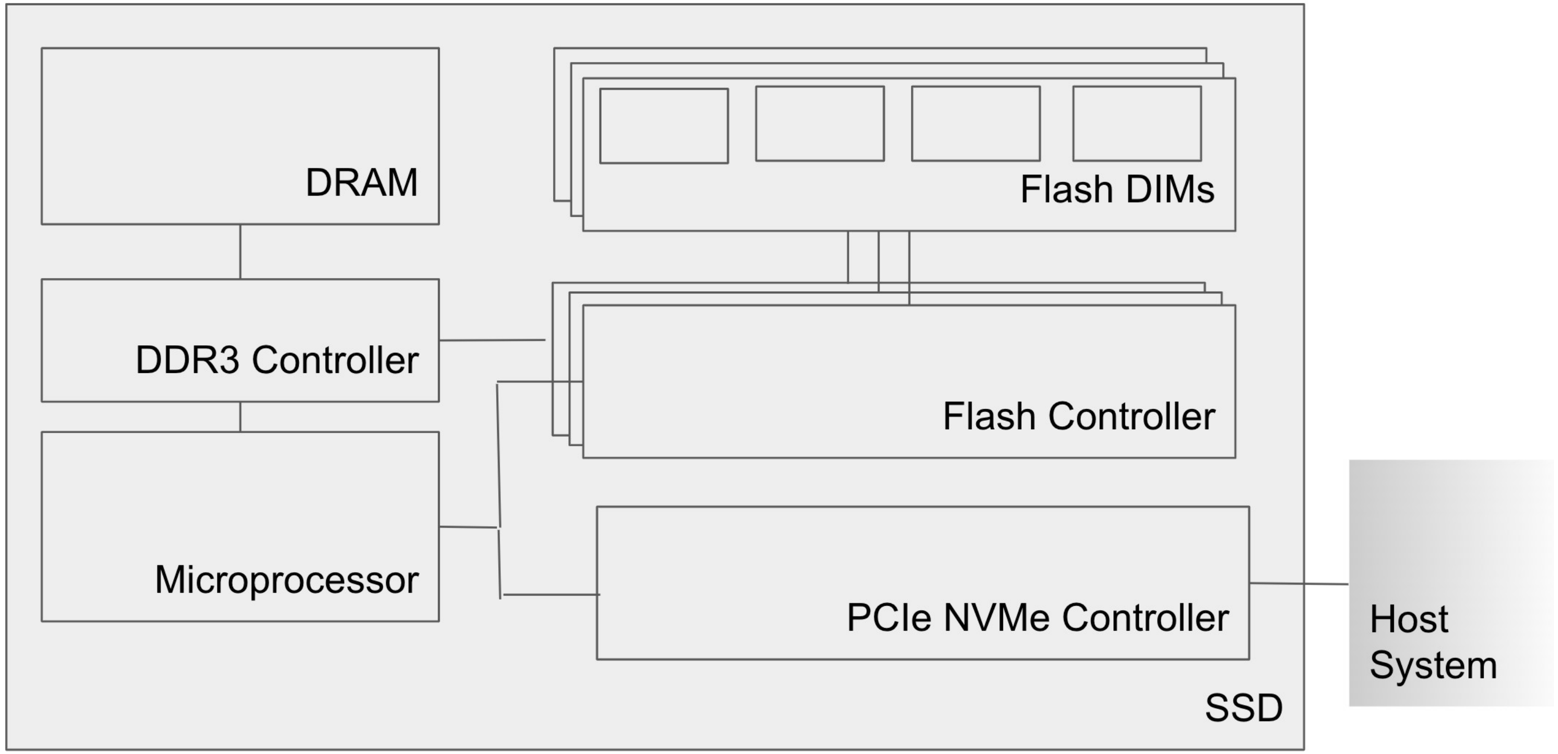
RecSSD [2]

[1] "Bandana: Using Non-volatile Memory for Storing Deep Learning Models", SysML 19, Eisenman et. al.

[2] "RecSSD: Near Data Processing forSolid State Drive Based Recommendation Inference", ASPLOS 2021, Wilkening et. al.

RecSSD: Efficient NDP for Recommendation

Question: What is NDP, why does it work, and when does it work?



RecSSD: Efficient NDP for Recommendation

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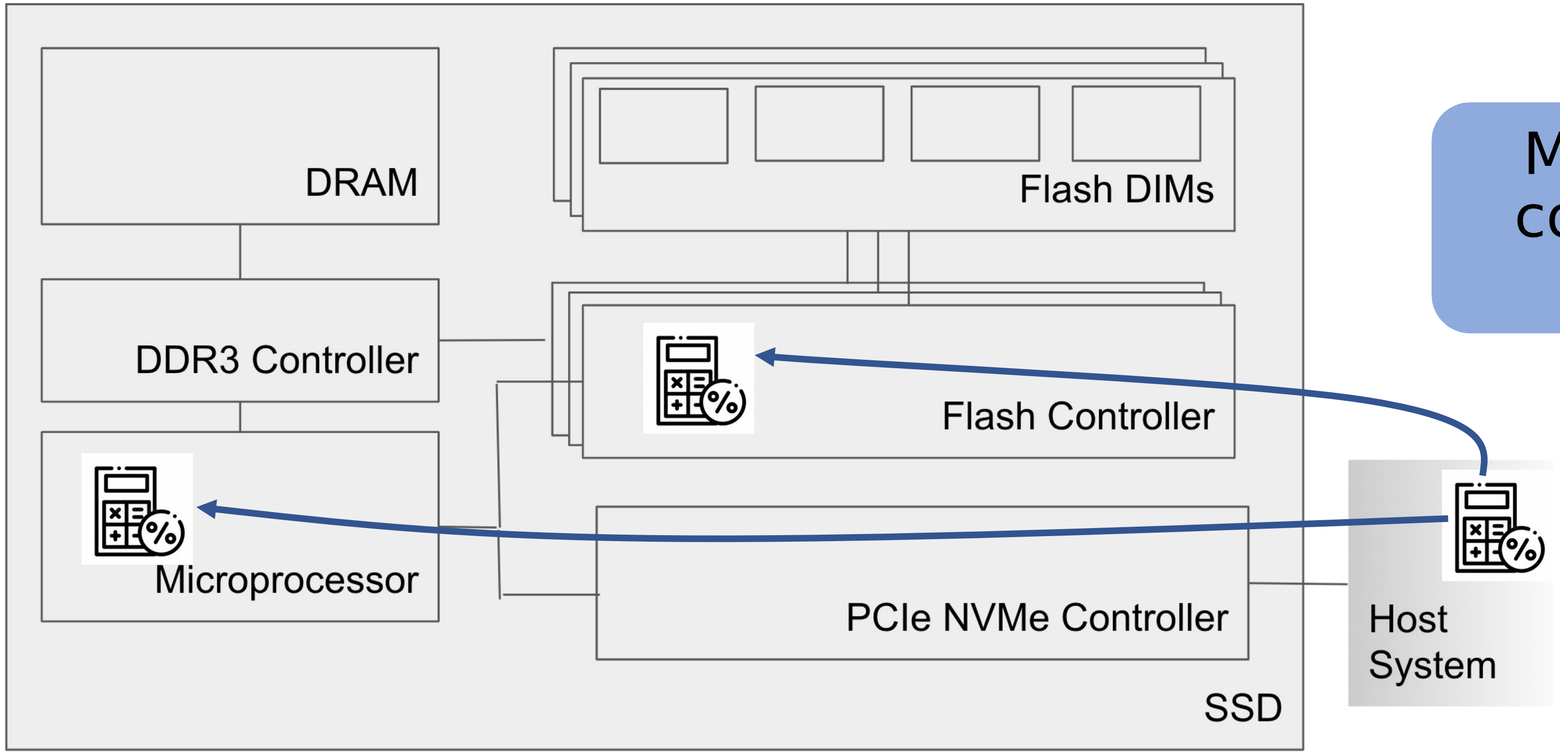

Move application specific computation closer to the data

RecSSD: Efficient NDP for Recommendation

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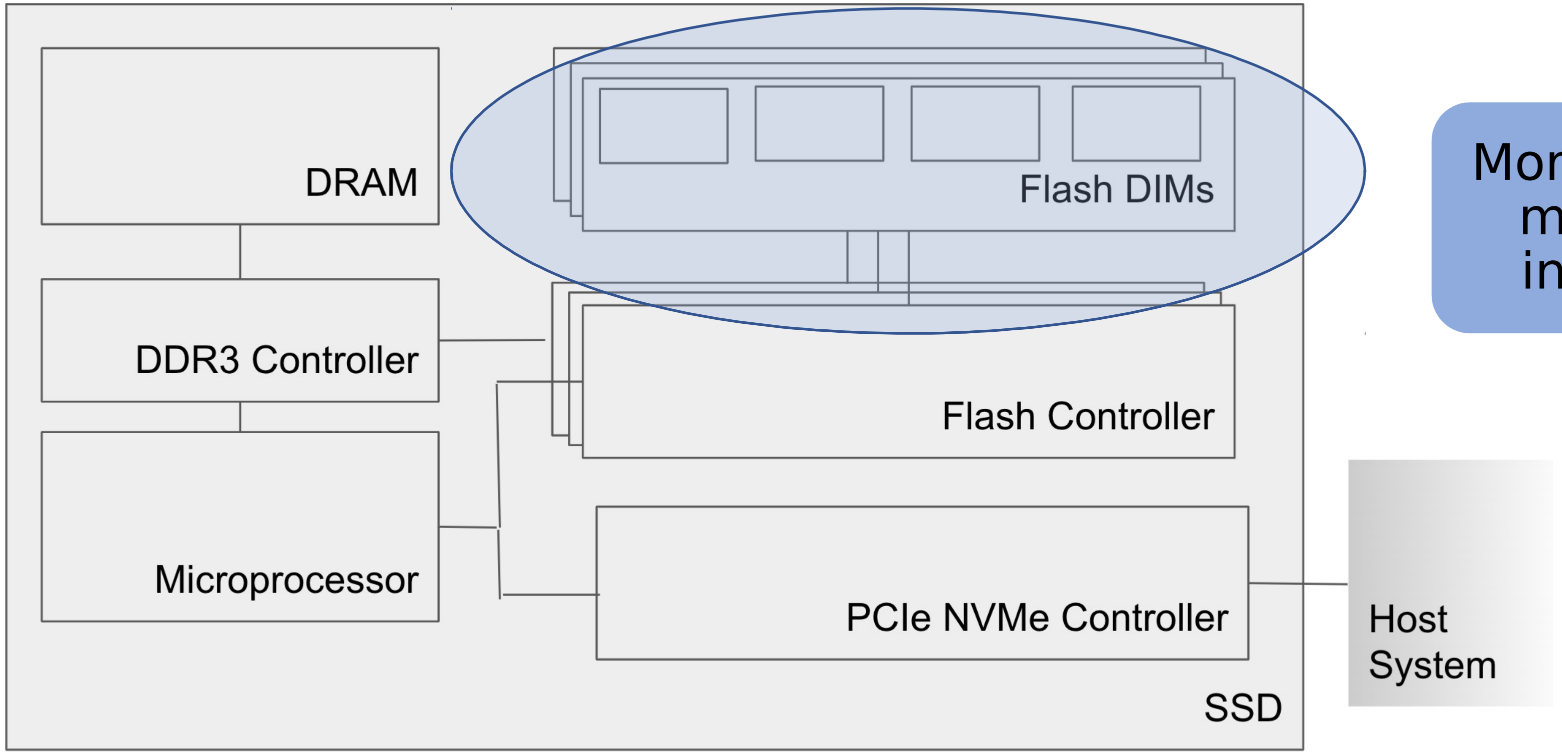
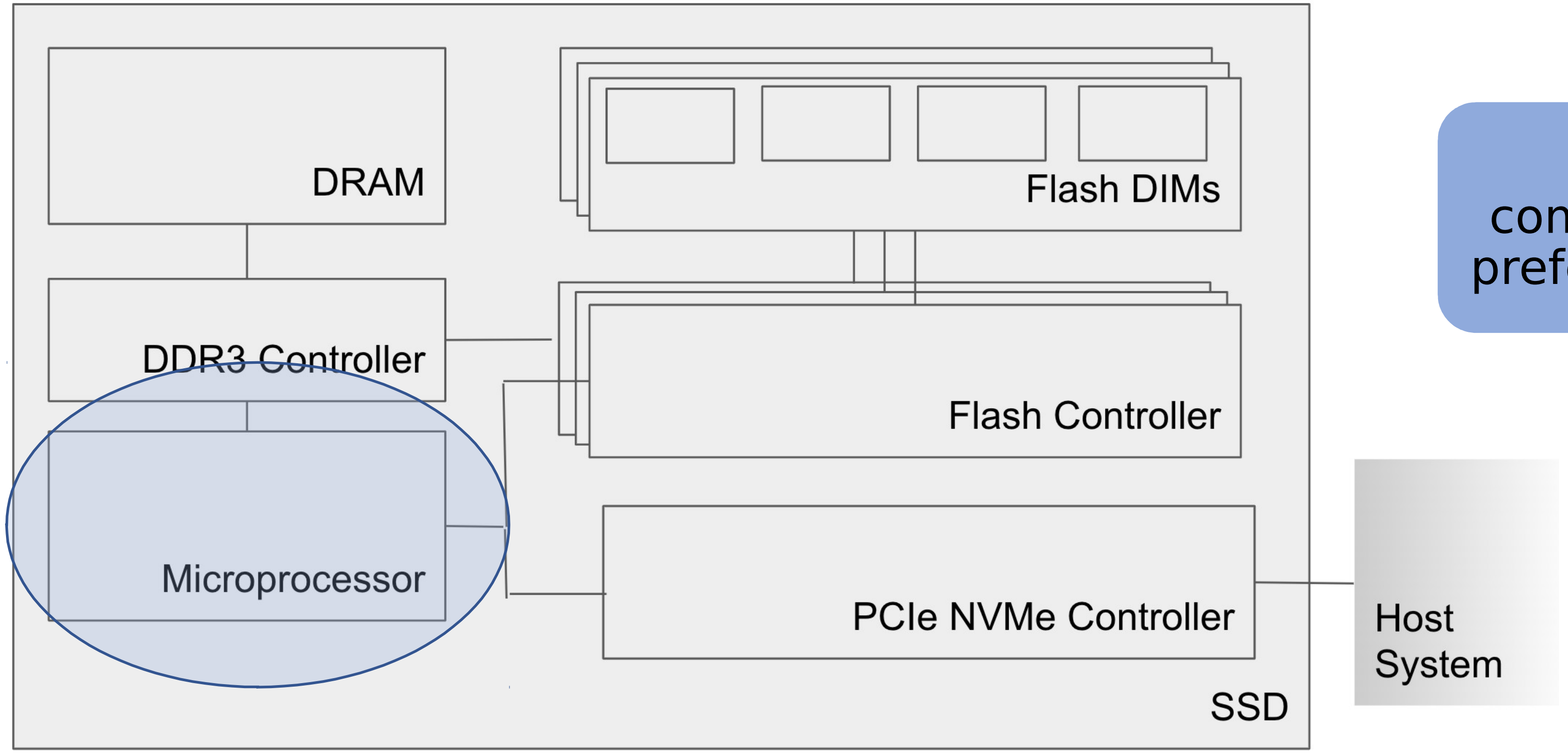


More efficiently leverage internal memory level parallelism, for increased internal bandwidth

RecSSD: Efficient NDP for Recommendation

Question: What is NDP, why does it work, and when does it work?



Requires data intensive, computationally light tasks, which preferably reduce to simpler results

RecSSD: Efficient NDP for Recommendation

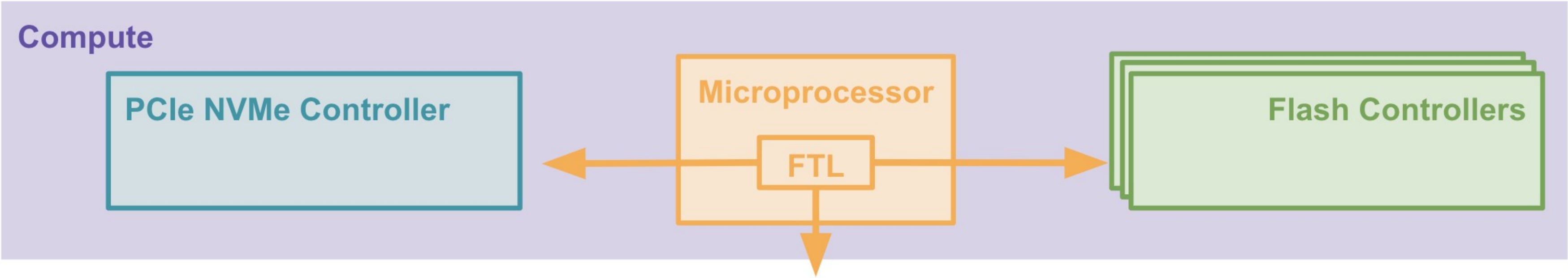
General Purpose NDP

- Built for a wide array of computational tasks
- Typically relies on highly customized hardware accelerators, SSD firmware, host drivers, and programming interfaces

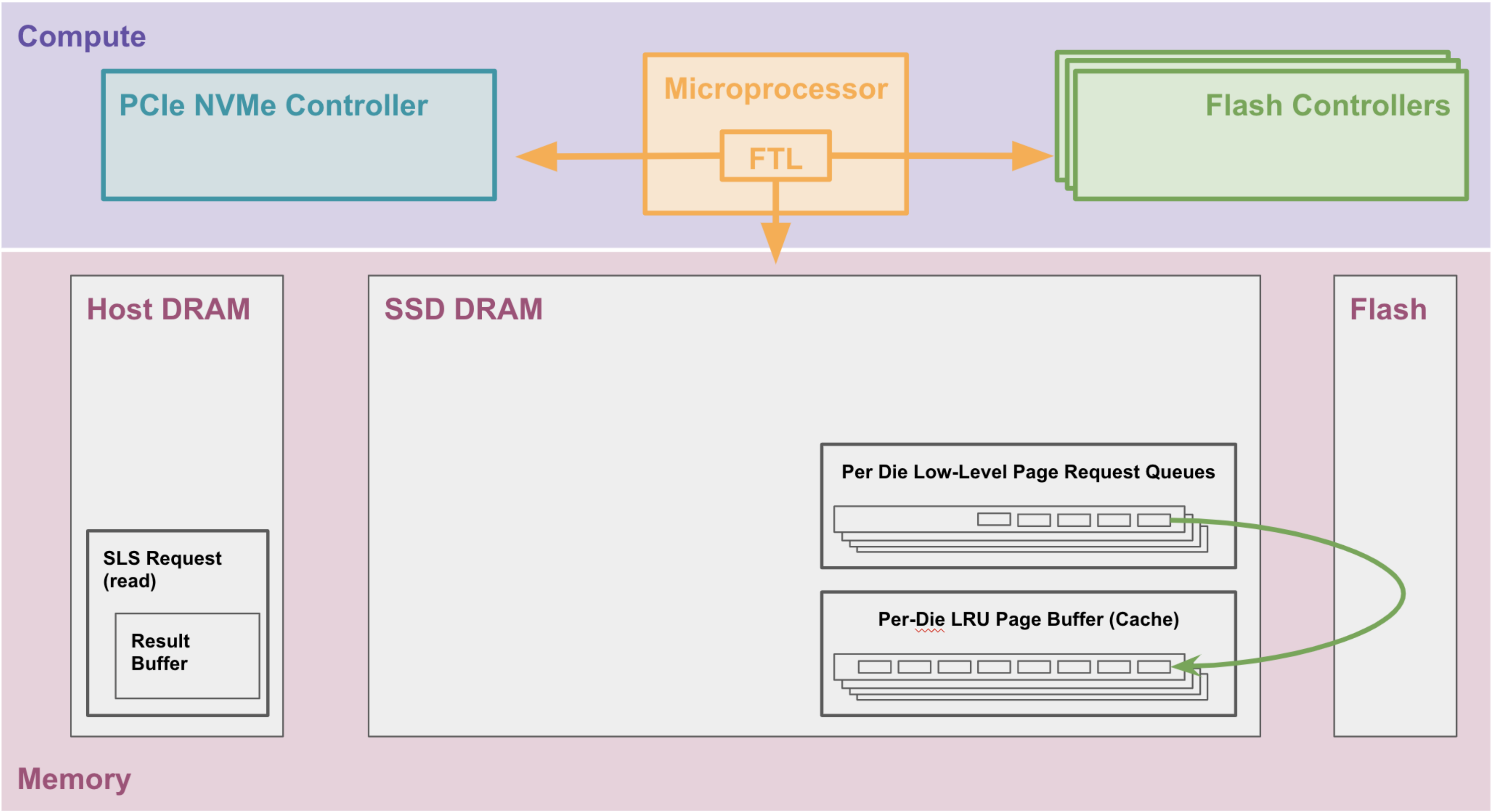
RecSSD

- Built for recommendation
- Uses commodity hardware
- Built entirely within the FTL
- Uses standard NVMe interfaces and minimal driver modifications
- Minimalist, cost efficient, low latency

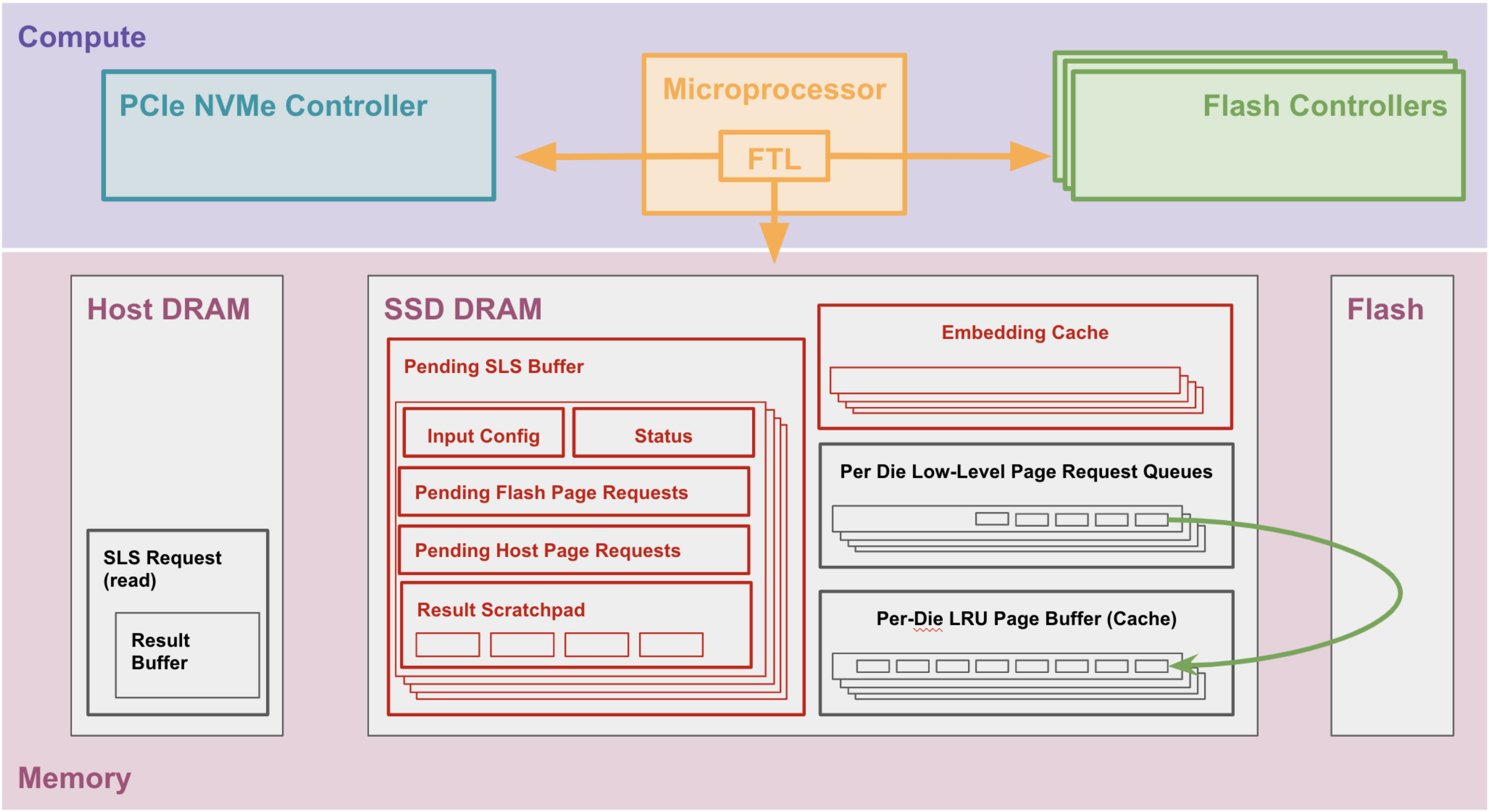
RecSSD Design Overview



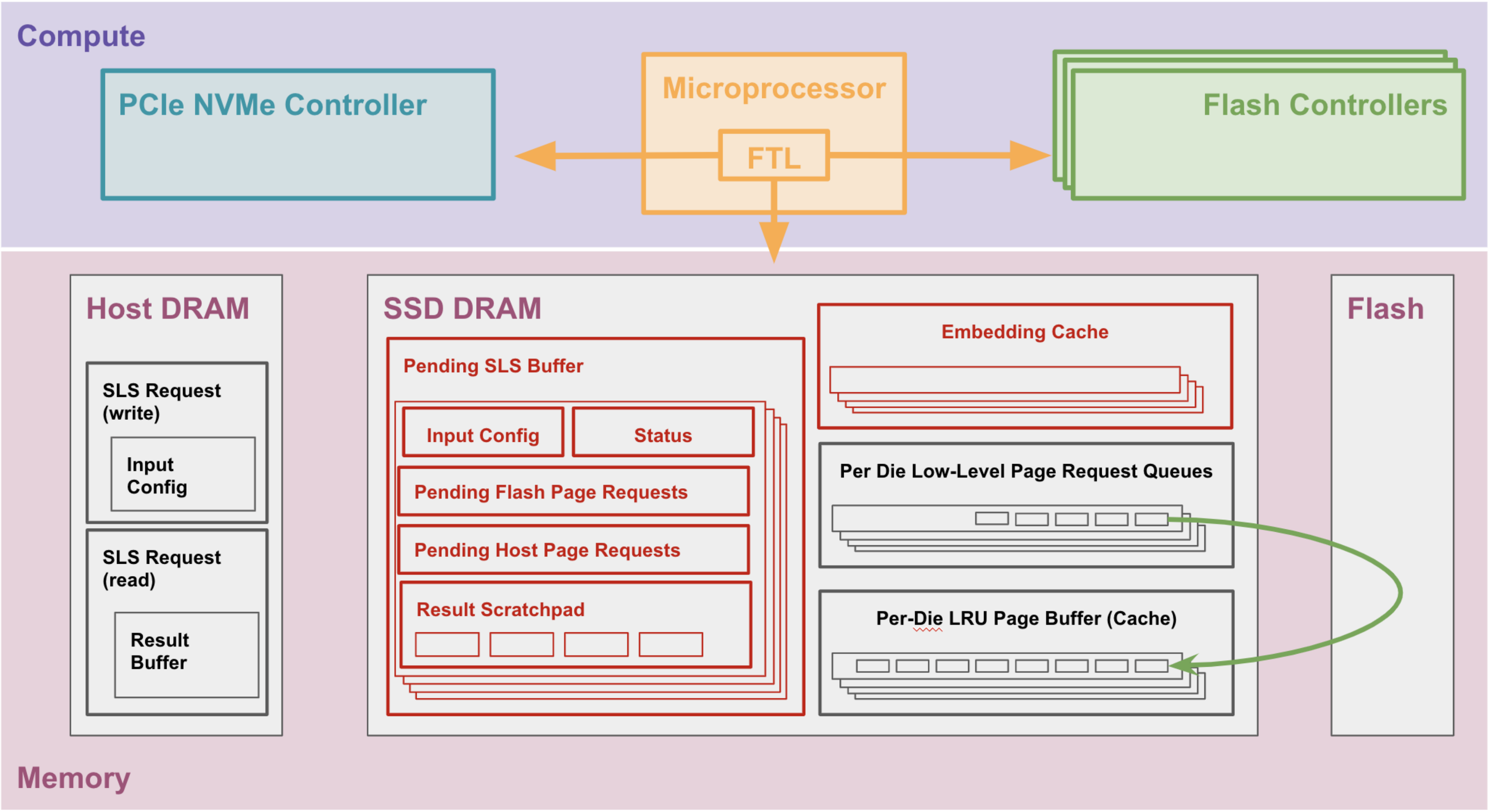
RecSSD Design Overview



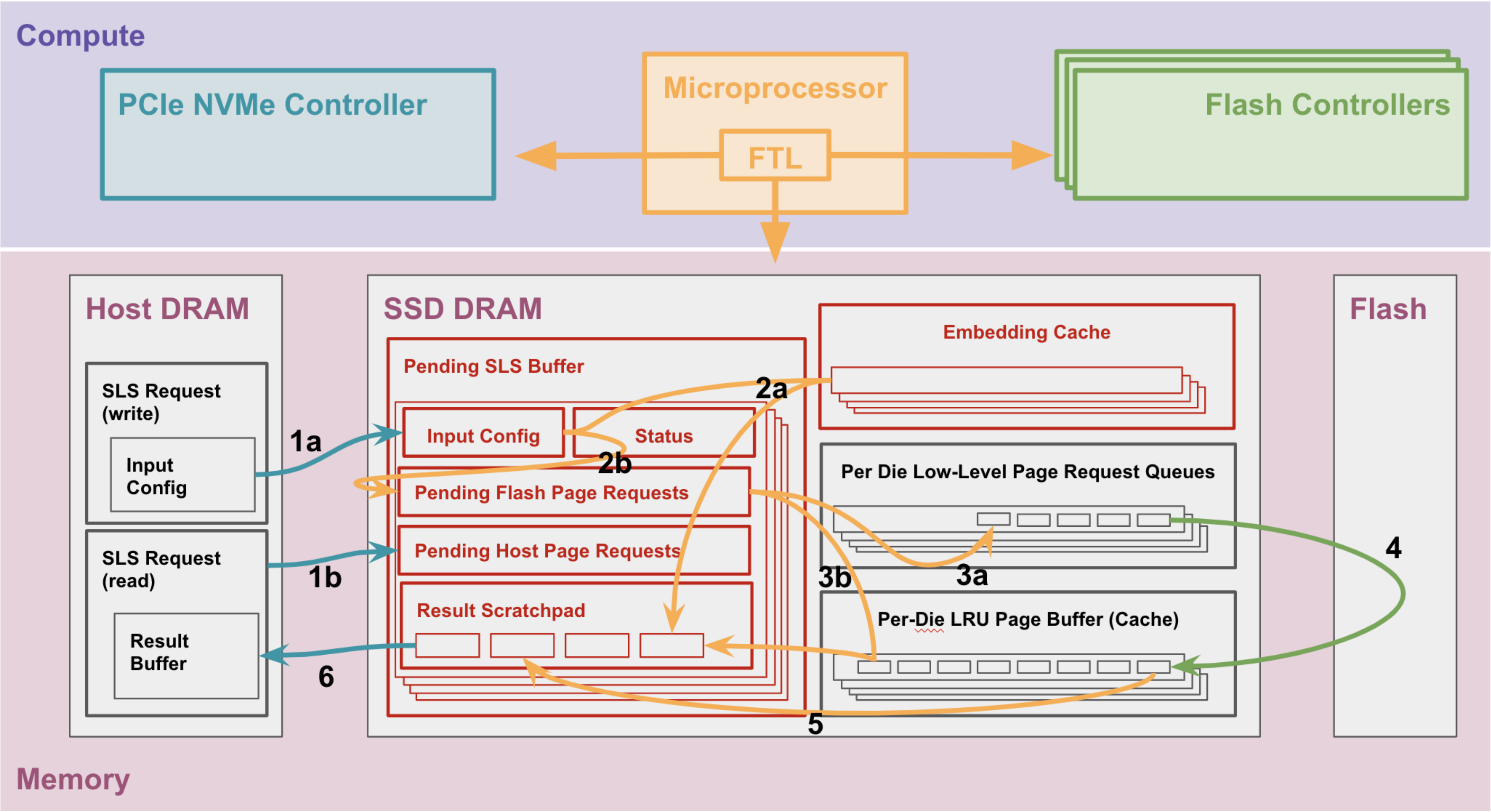
RecSSD Design Overview



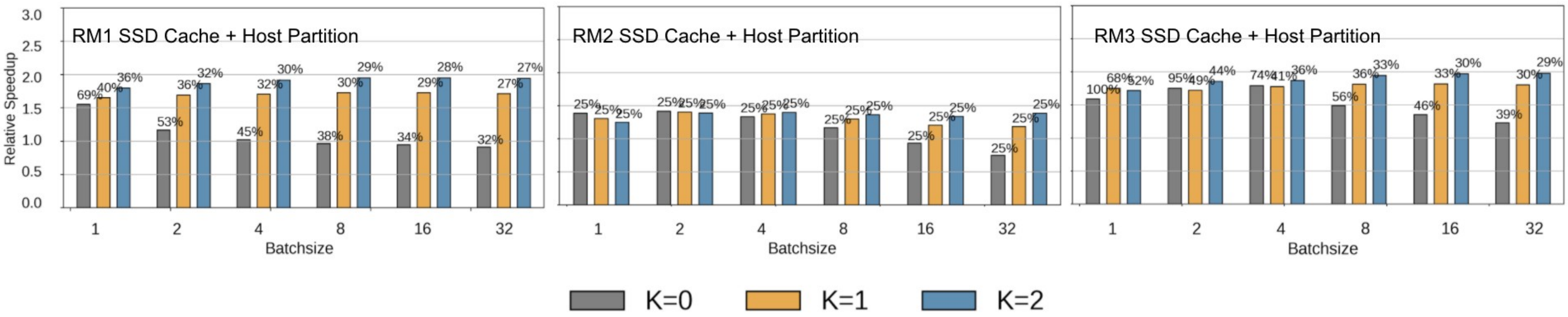
RecSSD Design Overview



RecSSD Design Overview



RecSSD Performance

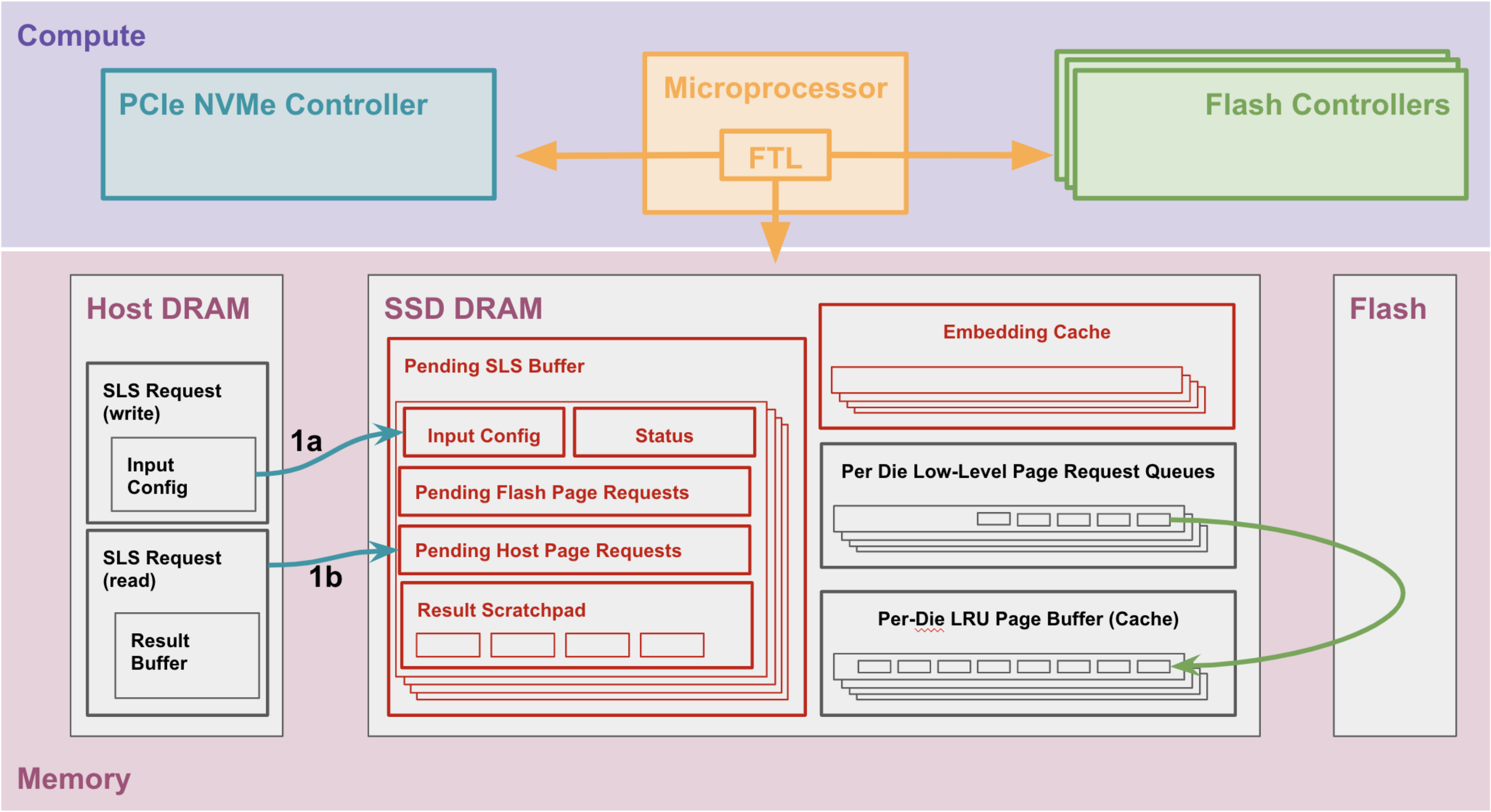


Up to 2x inference latency improvement alongside conventional caching techniques

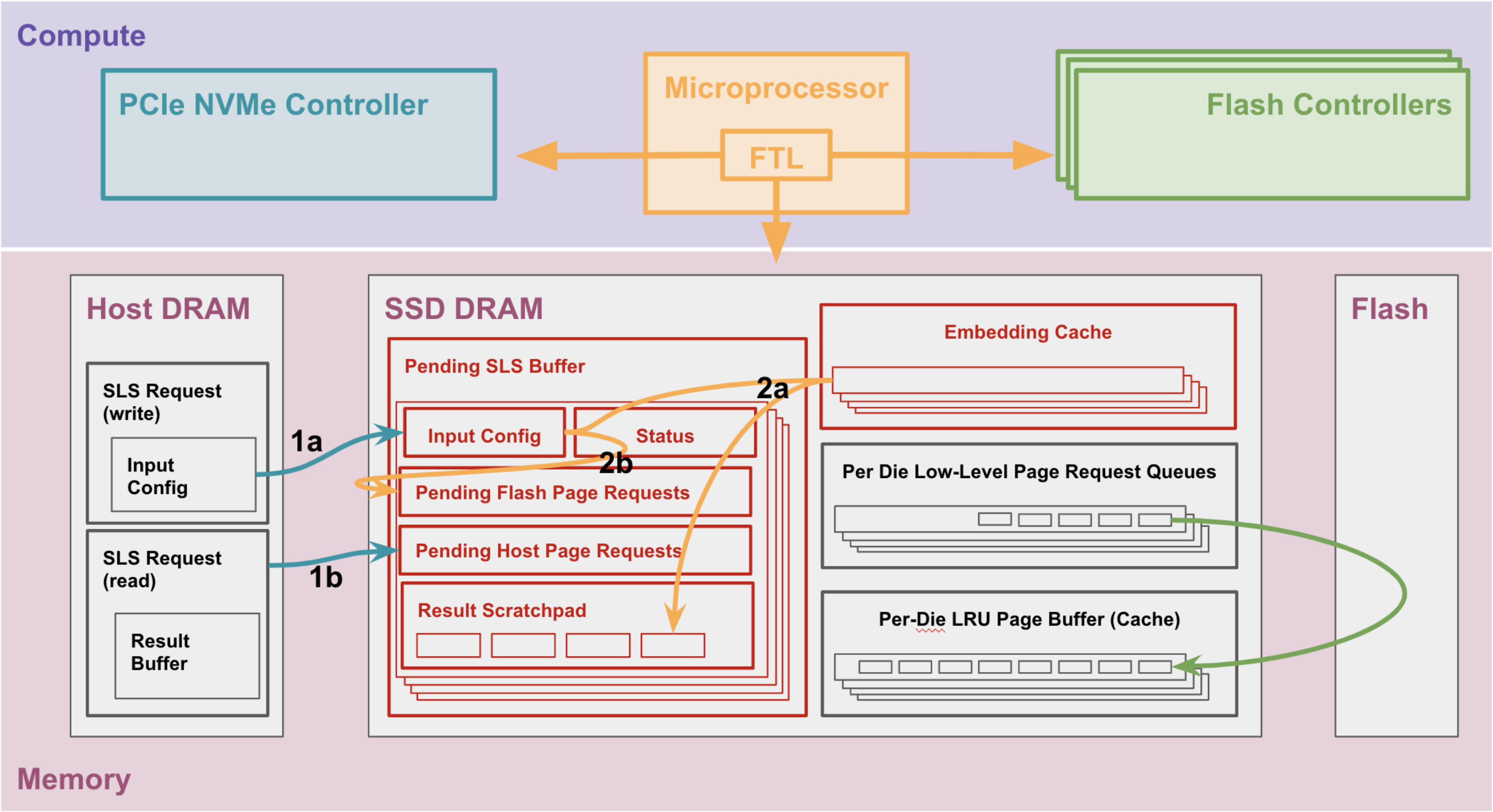
Thanks for listening!

Questions?

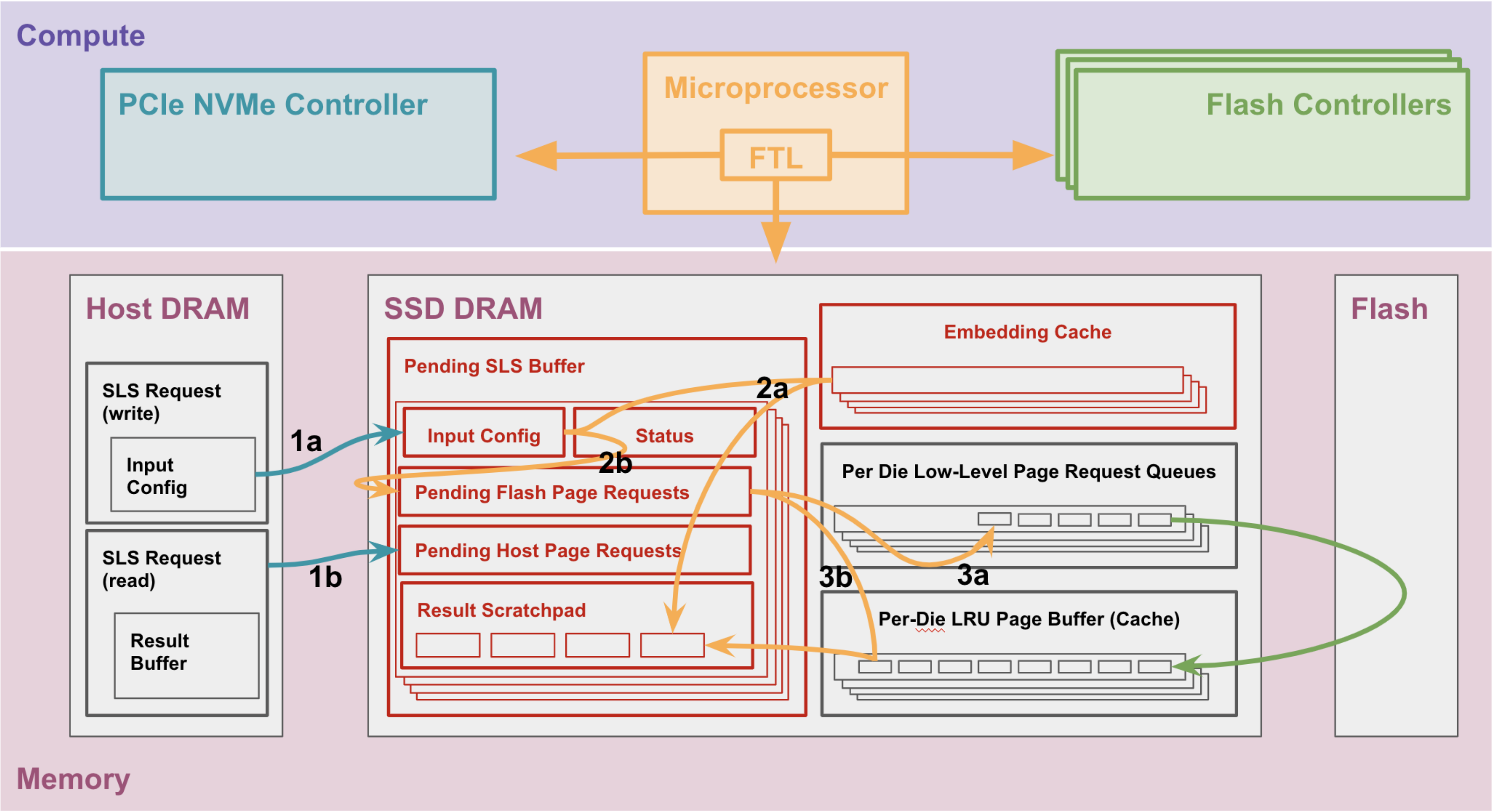
RecSSD Design Overview



RecSSD Design Overview



RecSSD Design Overview



RecSSD Design Overview