Hardware-Software Coordination for High-Performance Concurrent Data Structures with Near-Data-Processing

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Boston Area Architecture Workshop

Near-Data-Processing (NDP)

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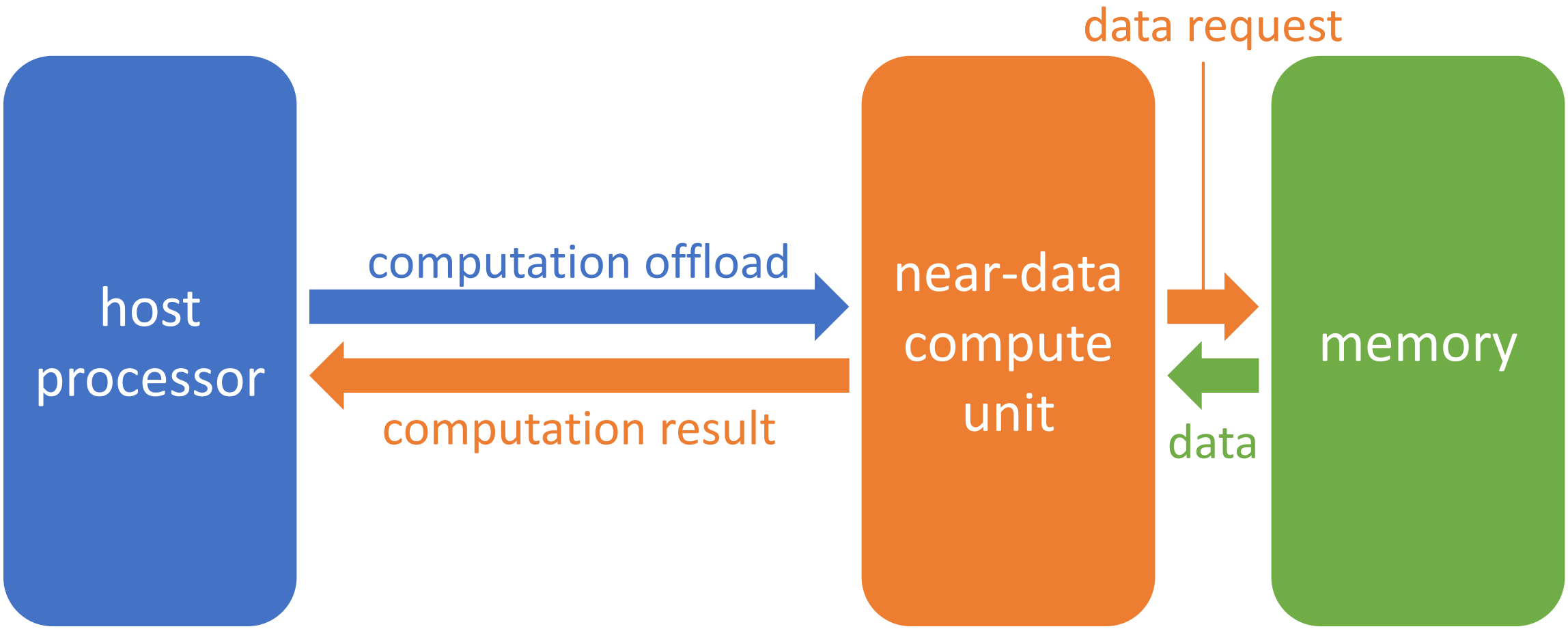

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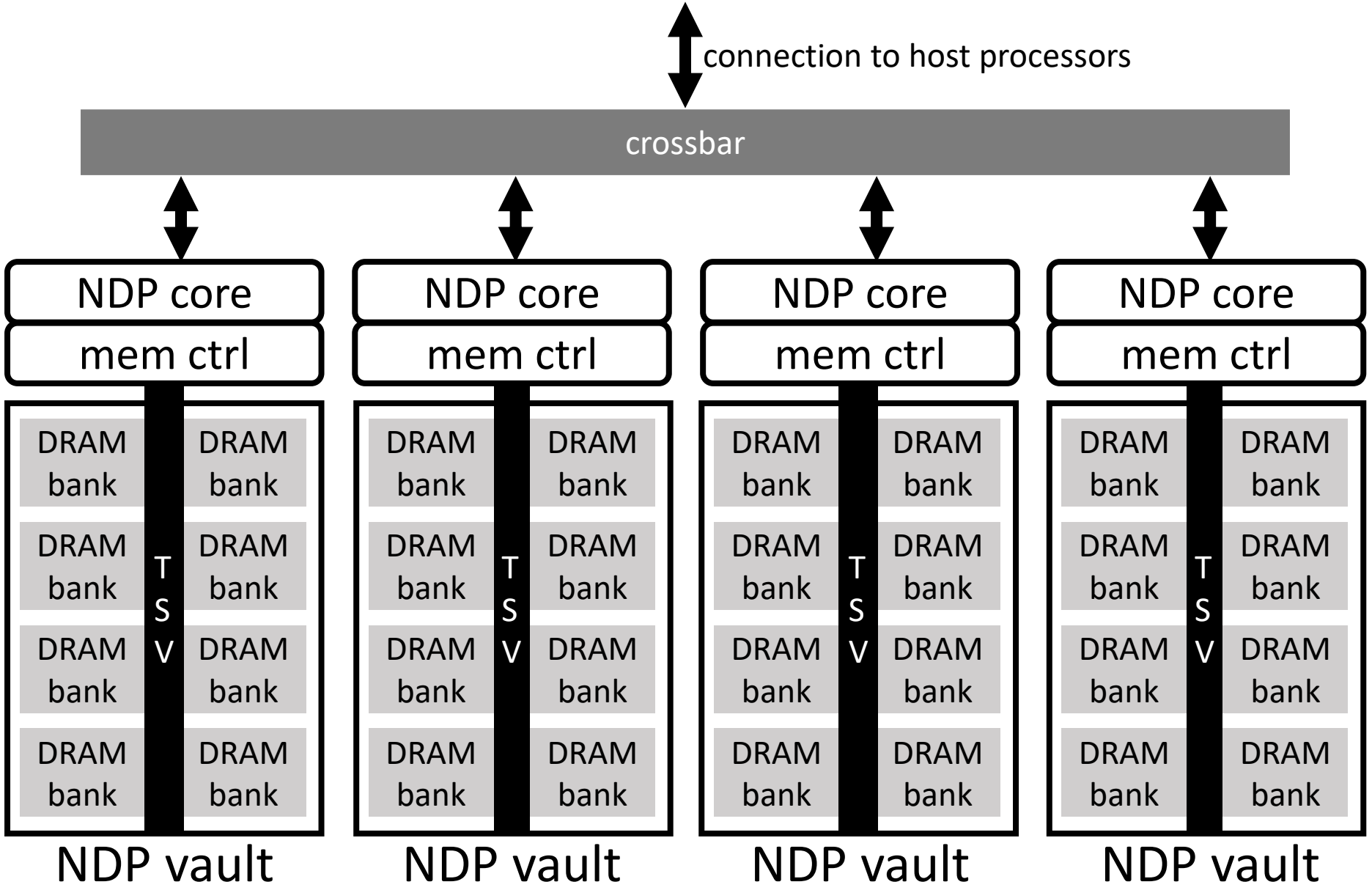

Concurrent Data Structures

- Bottlenecks on conventional architectures:
  - Poor cache locality (pointer-chasing data structures)
  - High-contention spots (contended data structures)

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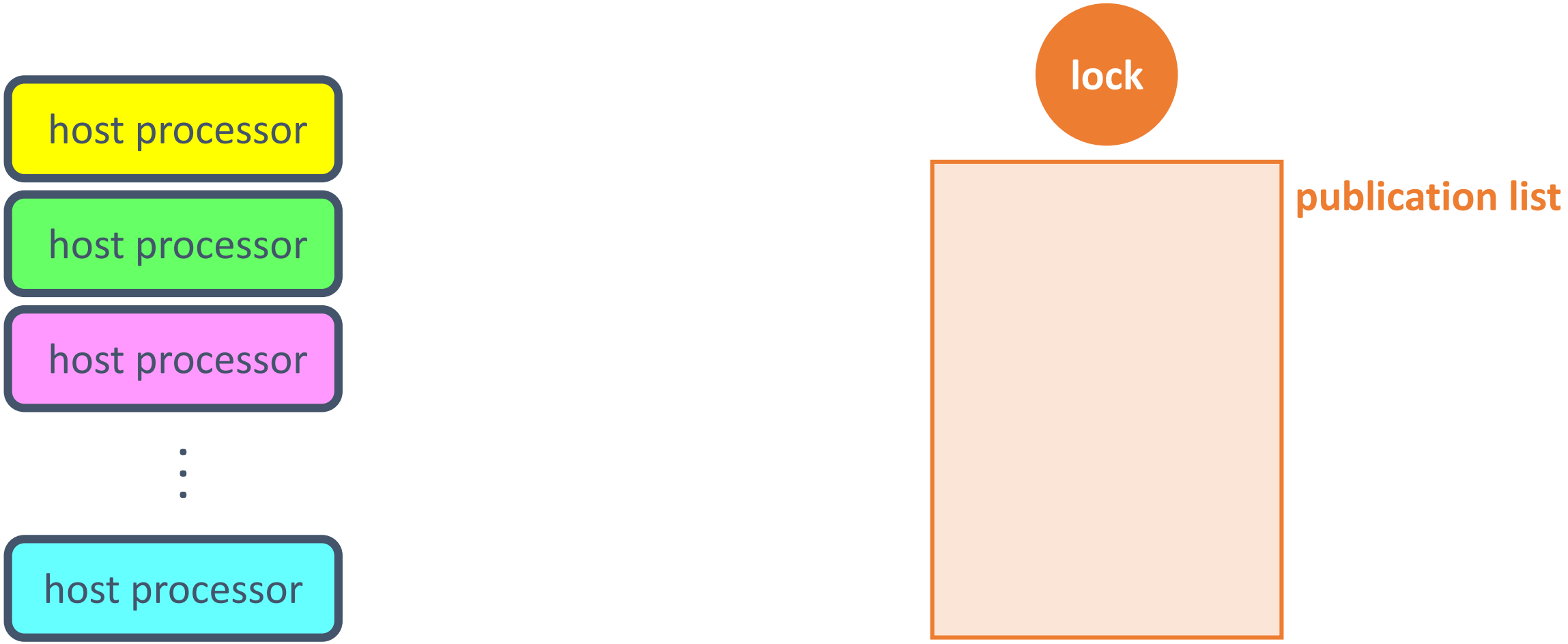
- Concurrency must be retained with NDP-based implementations

  Liu *et al*. SPAA 2017:
  - Naïve implementations on NDP will serialize data structure operations
  - Flat-combining techniques suggested

Flat-Combining (FC) Hendler *et al*. 2010



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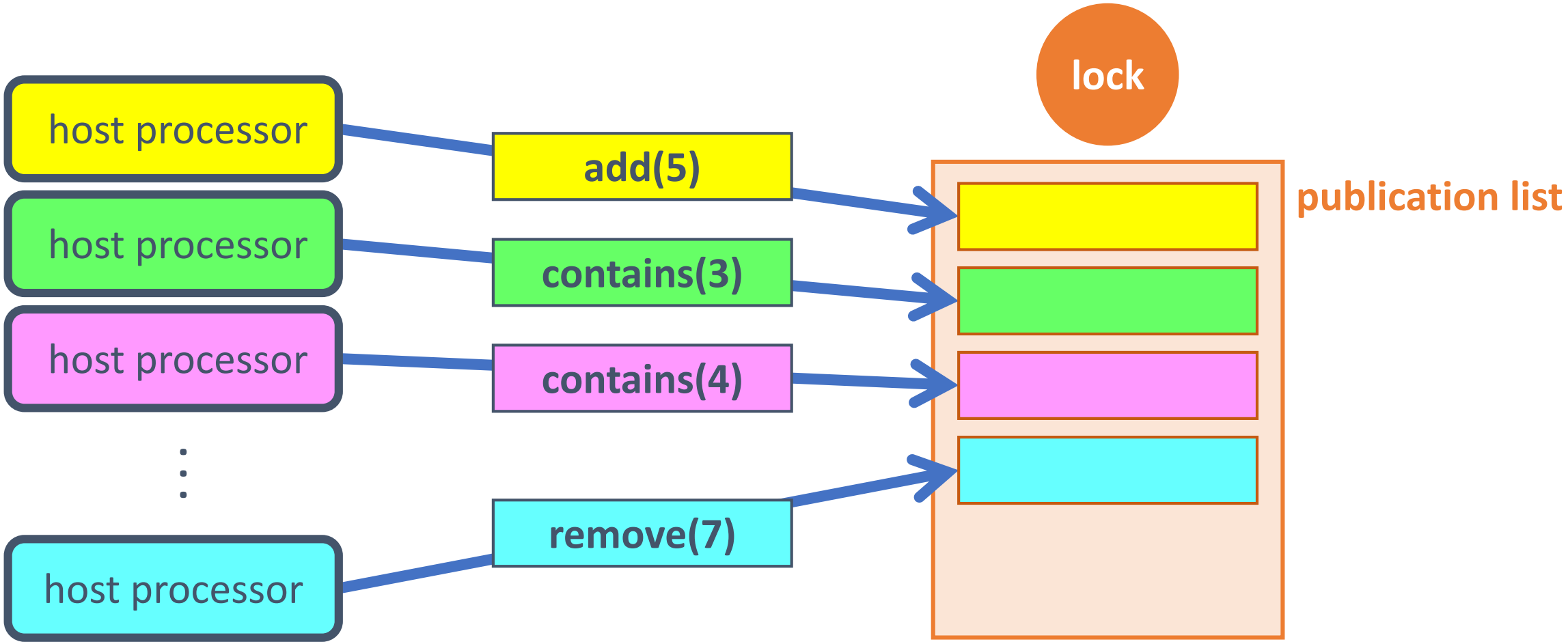

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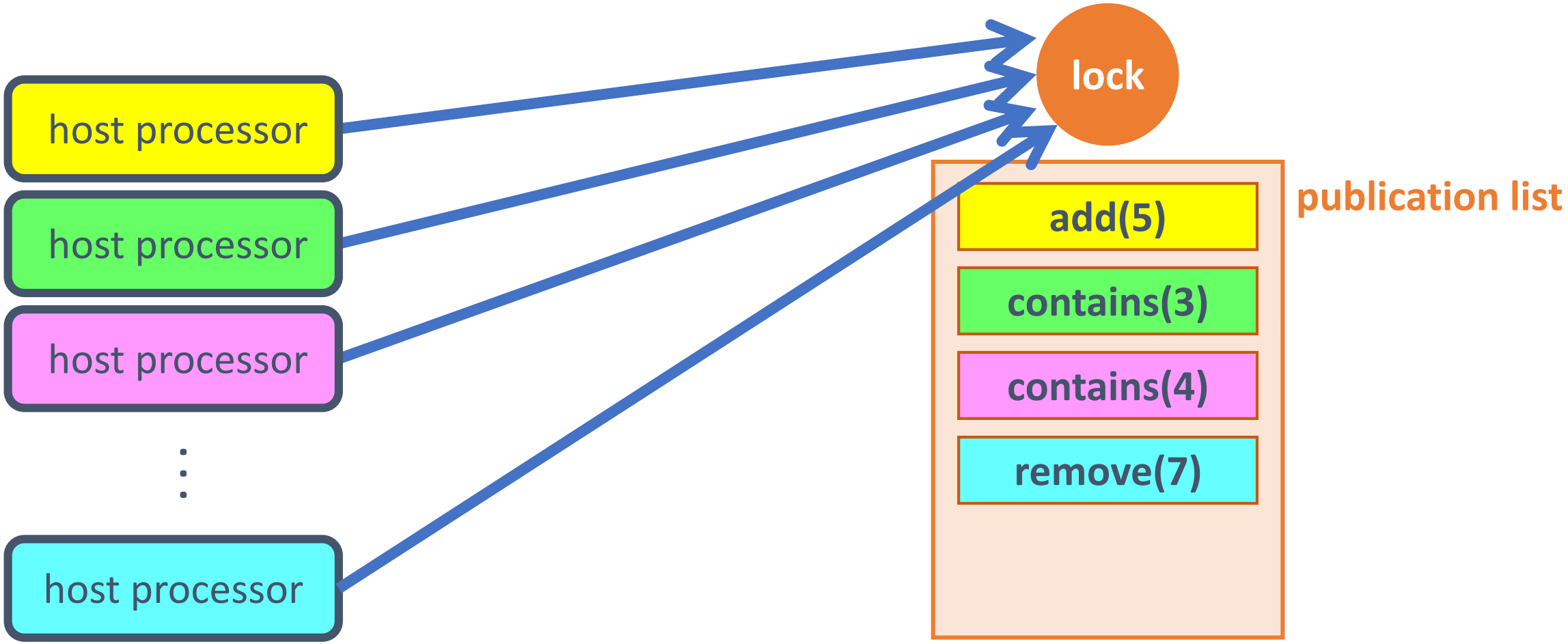

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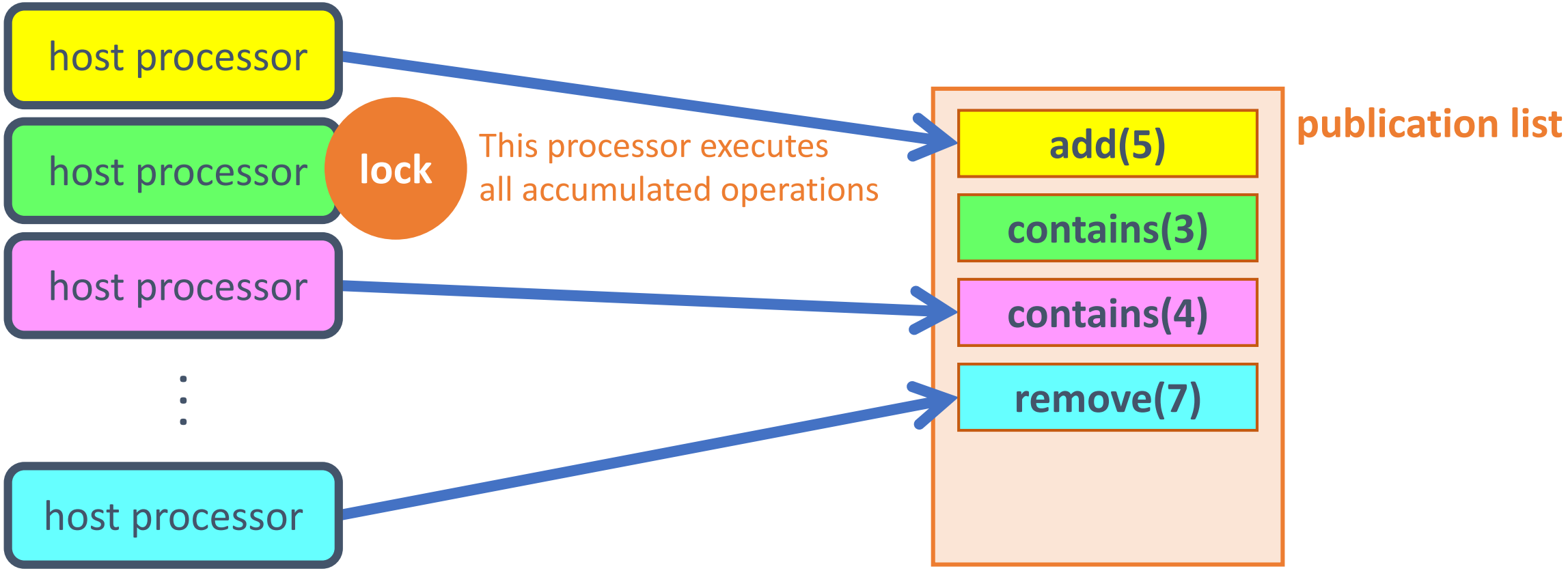
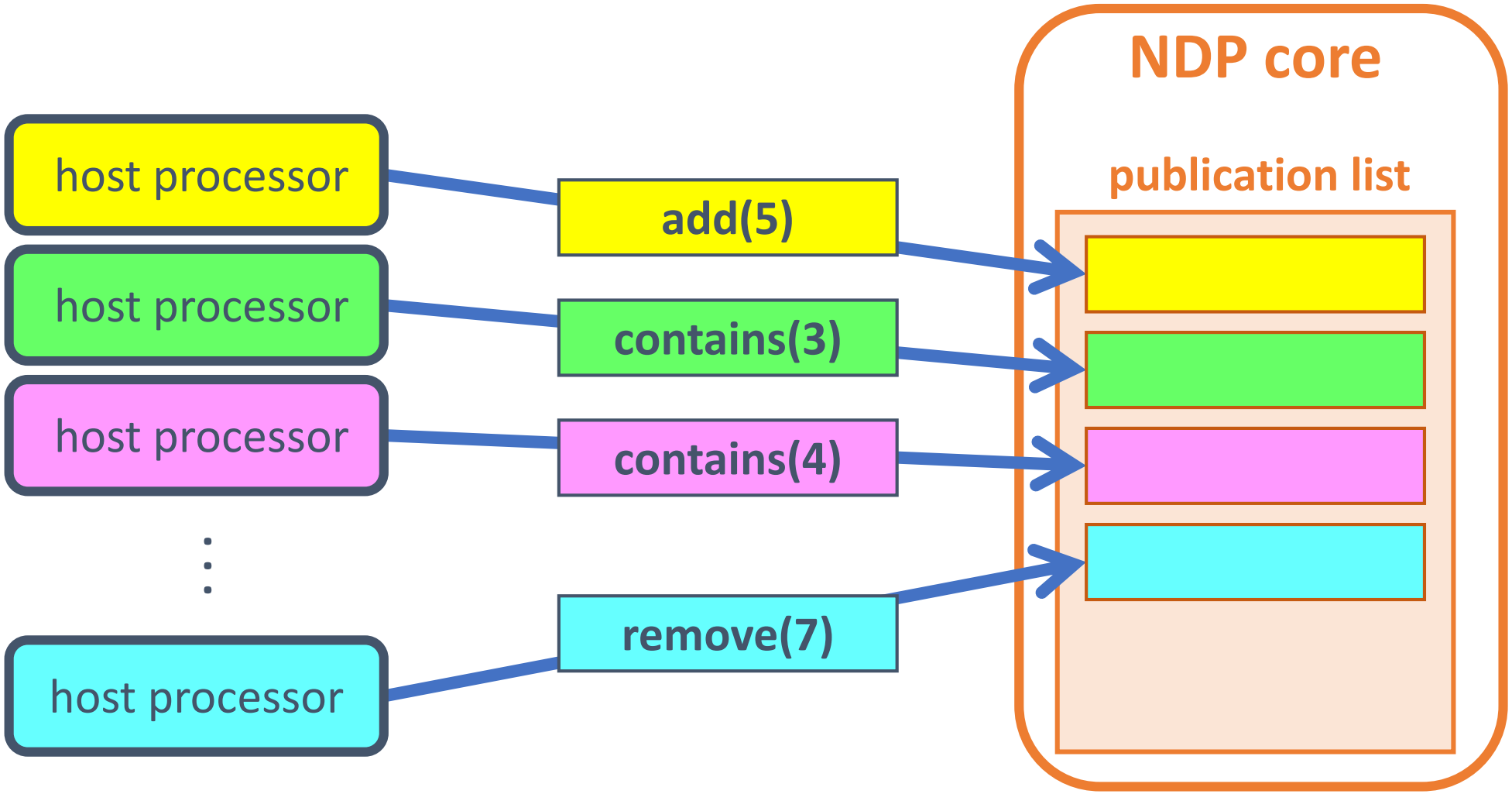
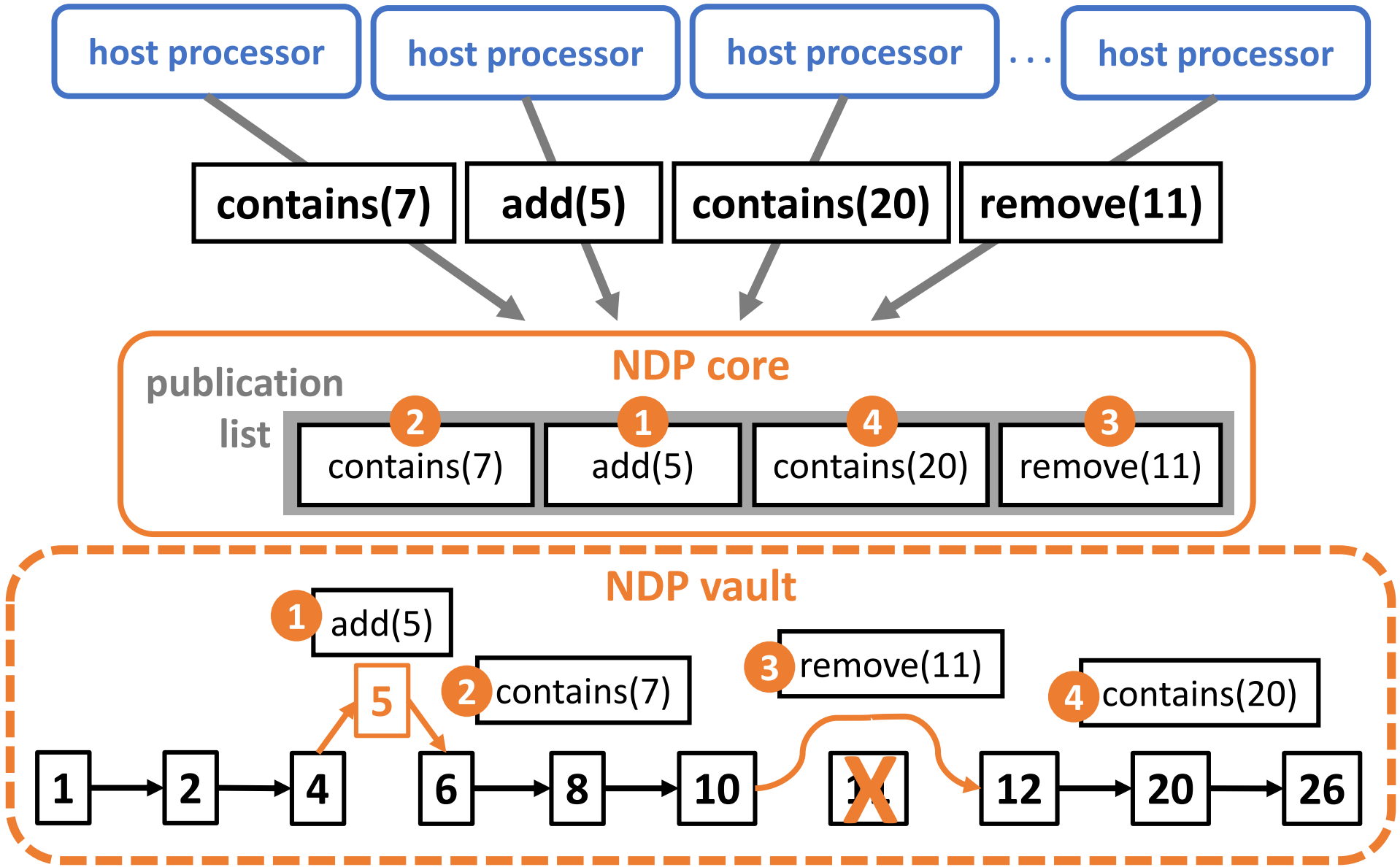


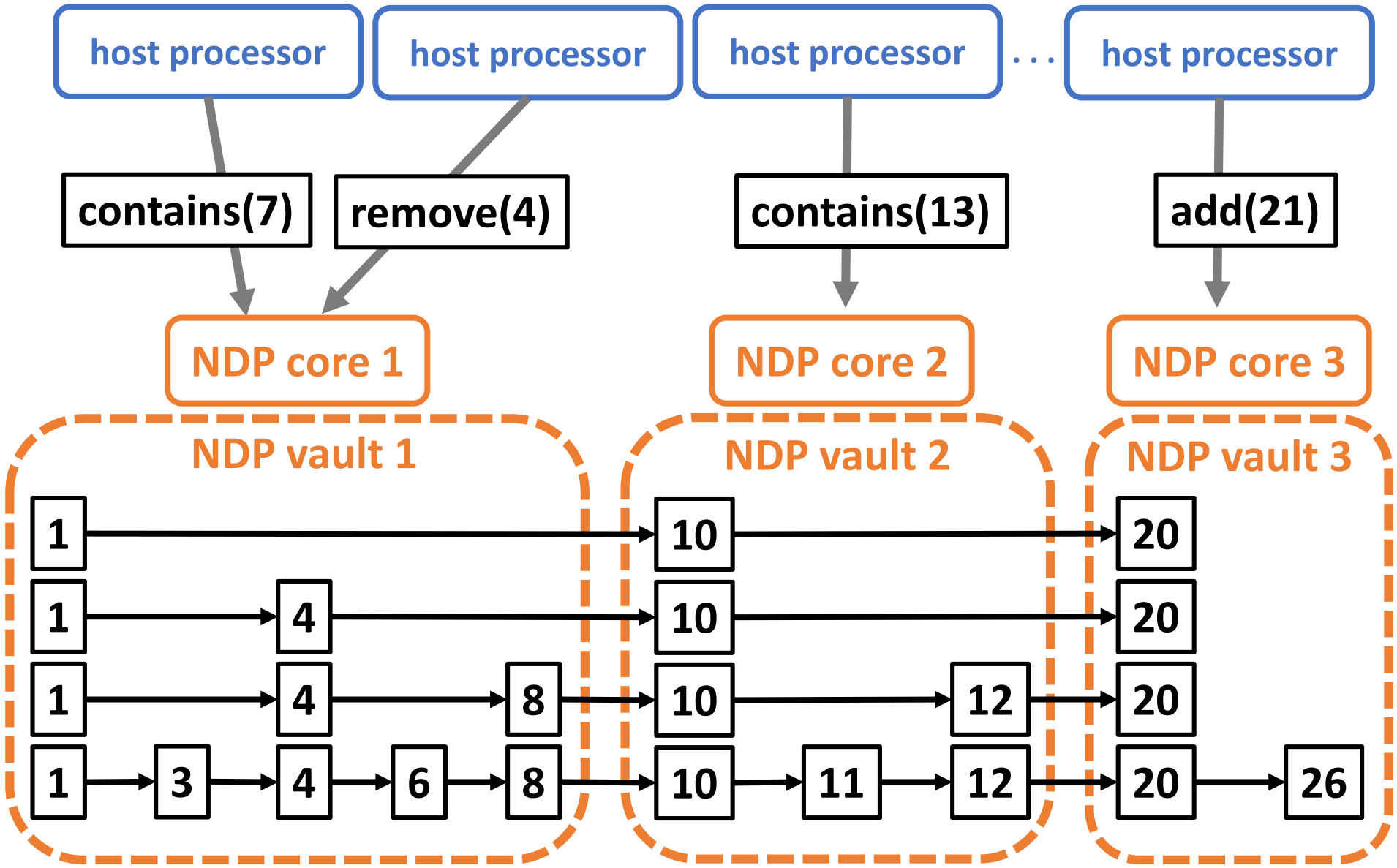
Flat-Combining with NDP Liu *et al*. 2017



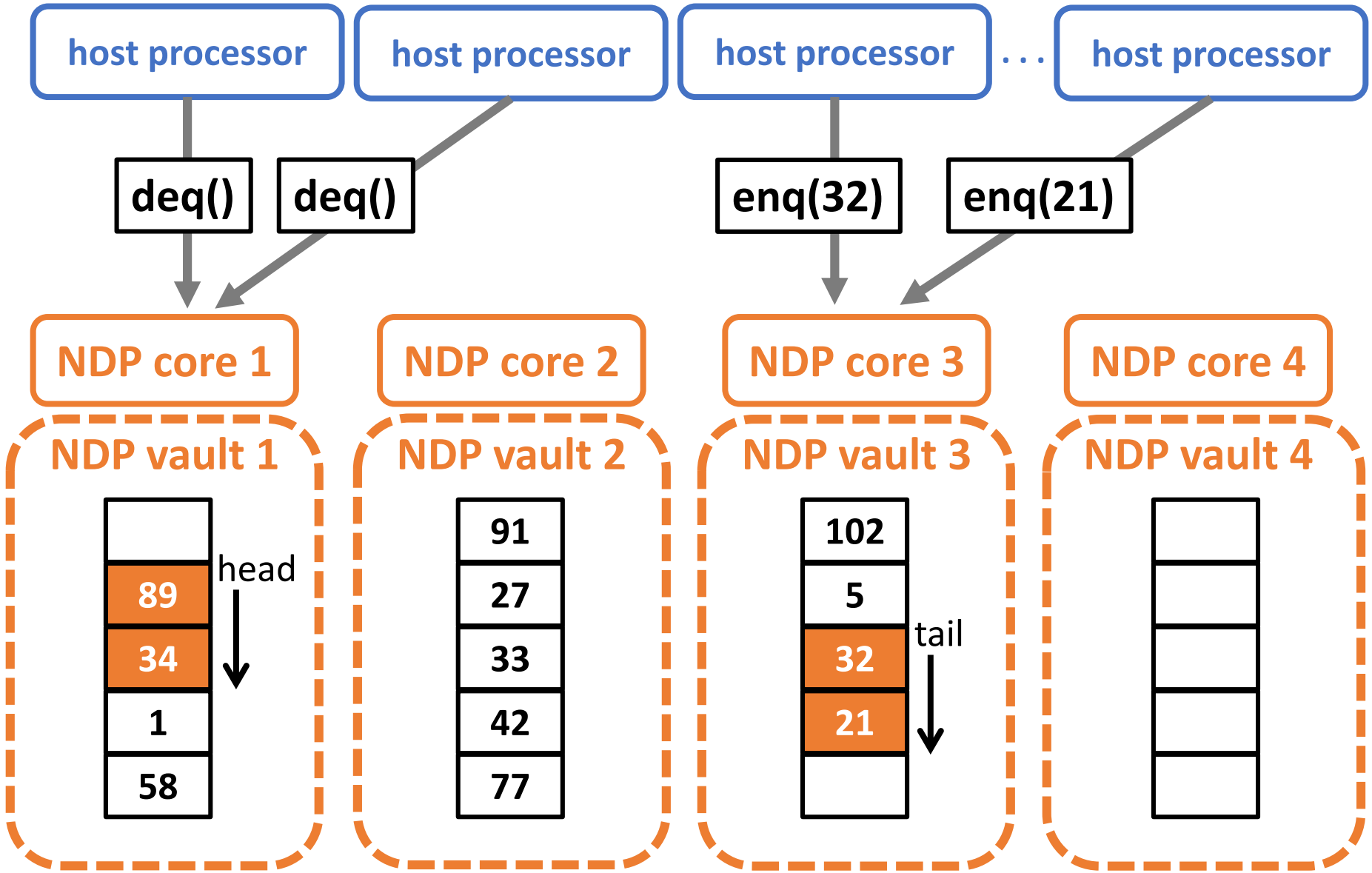
NDP-based Linked-List Liu et al. 2017



NDP-based Skiplist Liu et al. 2017



NDP-based FIFO Queue Liu et al. 2017



Limitations of Prior Work

Relied only on theoretical analysis with simple assumptions:

1. Overlooked cache impacts in host-based data structures
2. Overly optimistic assumptions on NDP core's data access

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NDP does not magically remove all DRAM access latencies!!

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Lightweight hardware changes significantly improve NDP-based data structure performance.

DRAM Access Latency

linked-list node definition:

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struct node {
   uint32_t key;       // 4 bytes
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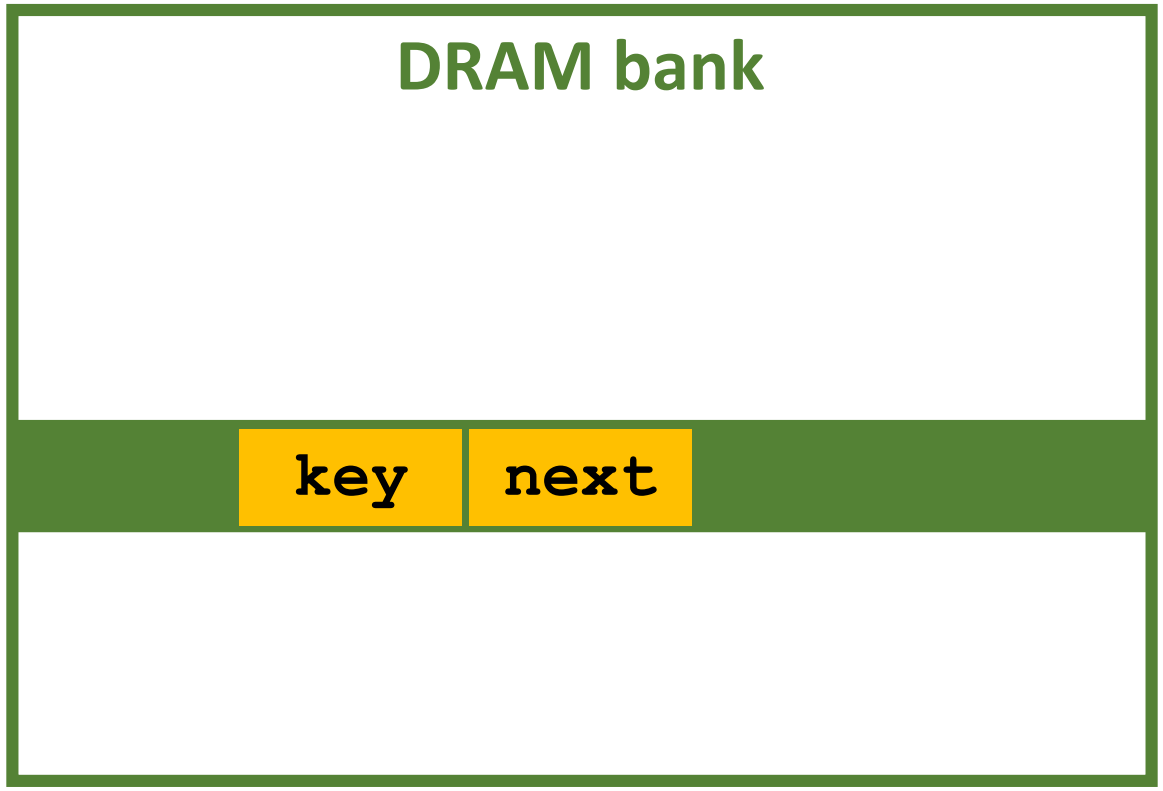

DRAM Access Latency

linked-list traversal:

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while (curr_node->key < param){
   curr_node = curr_node->next;
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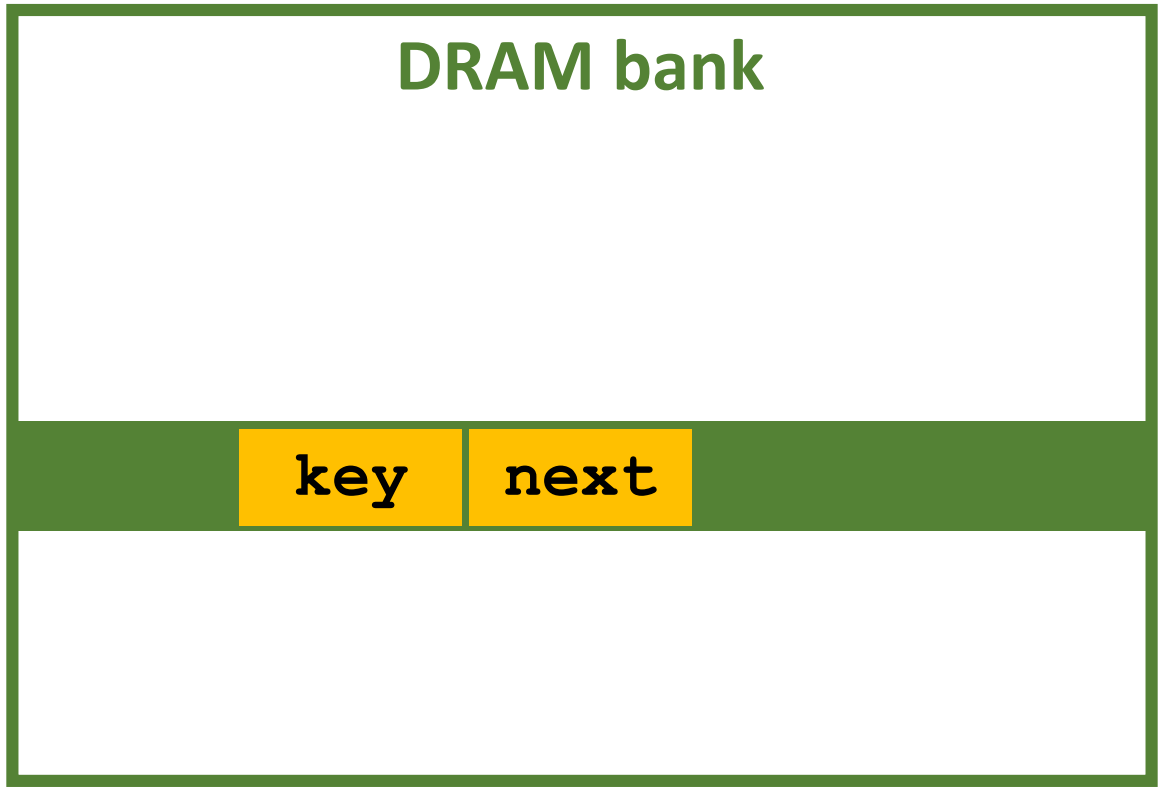

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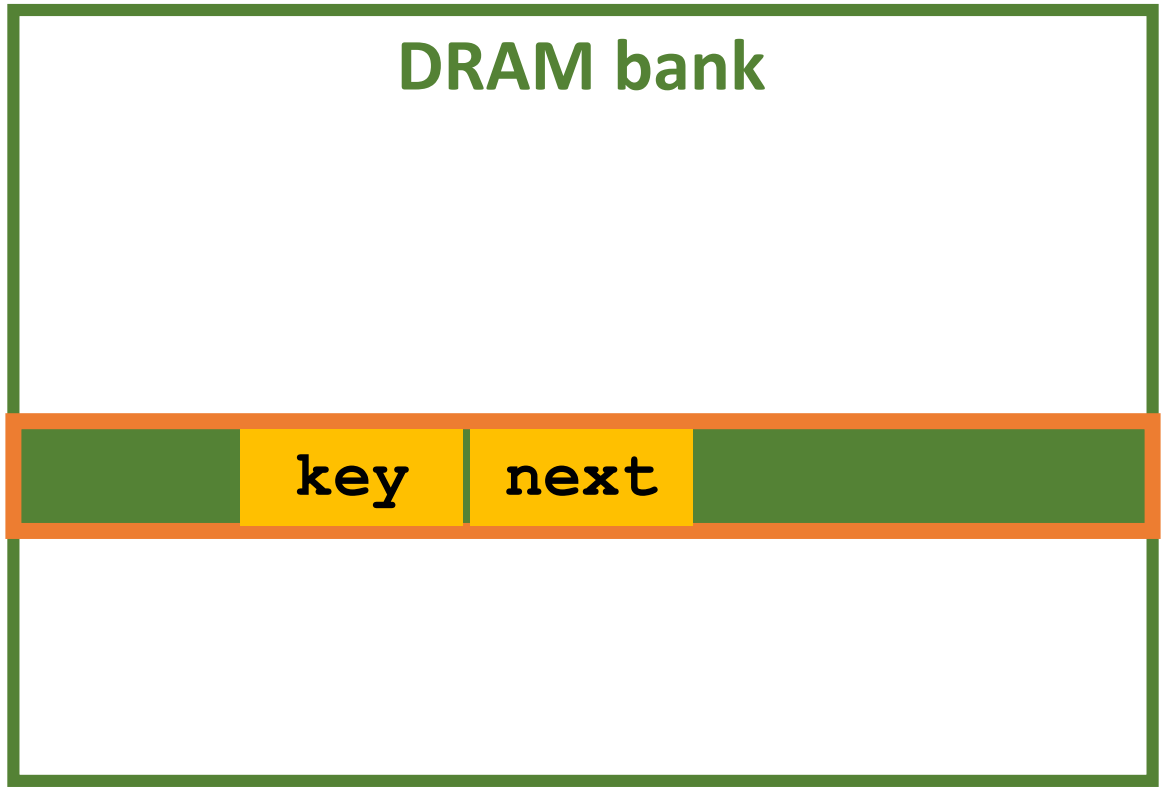
1. activate row containing `node->key`



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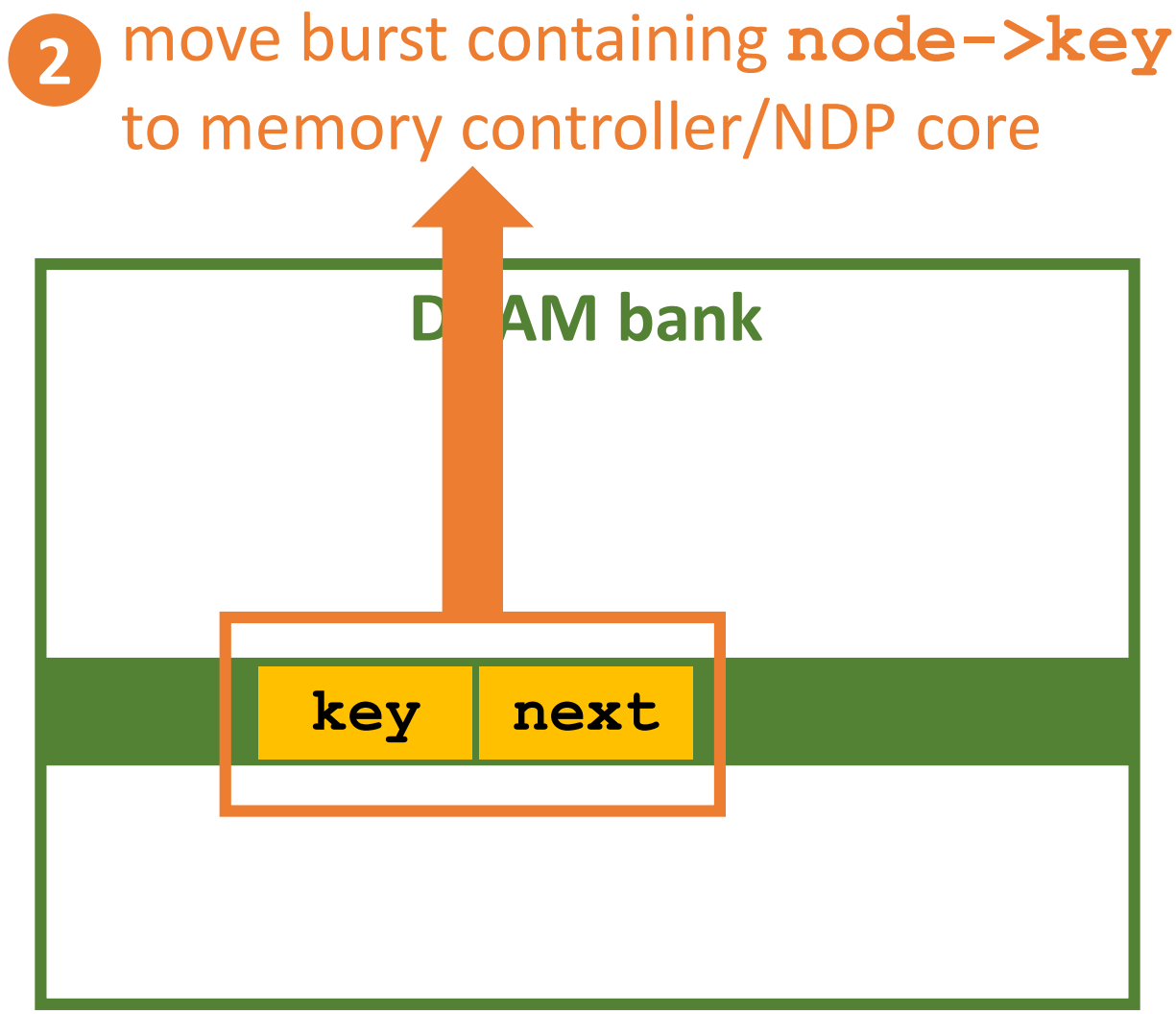

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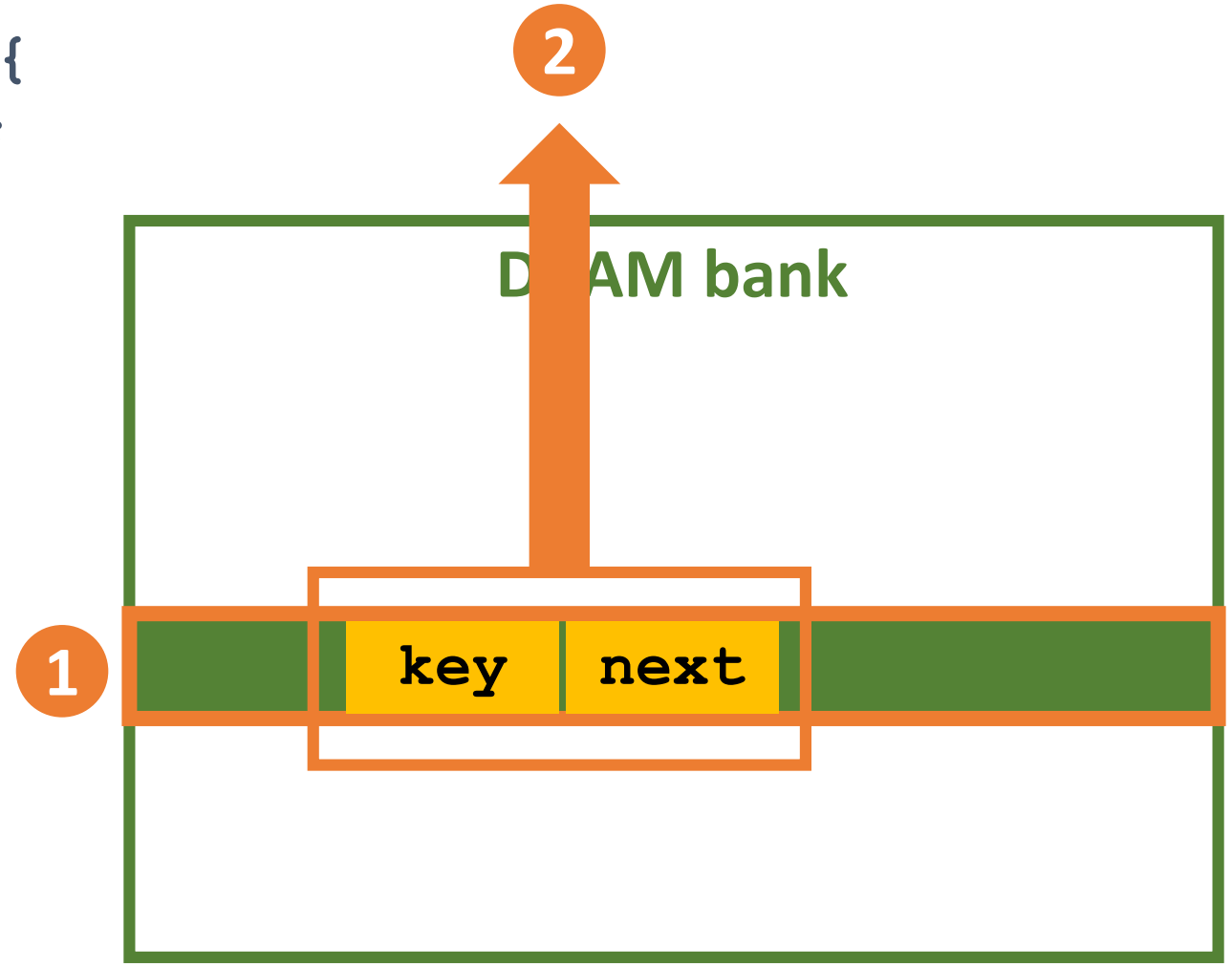
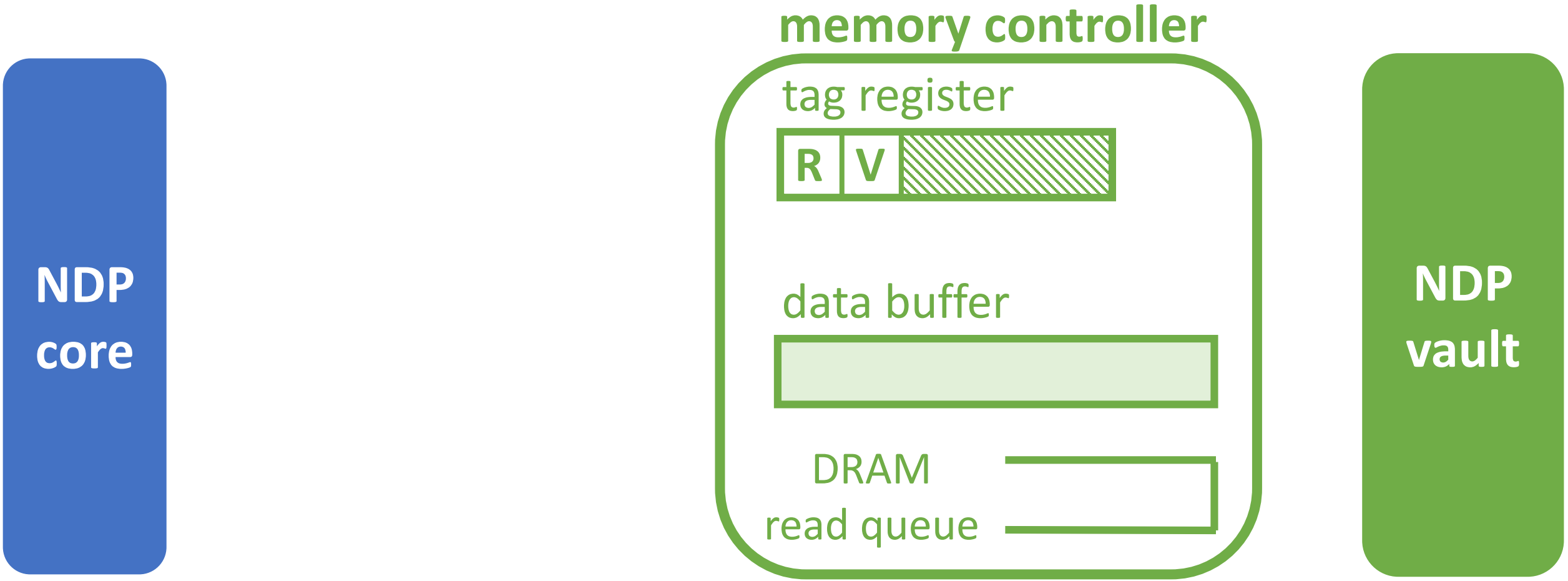
1, 2 repeated for `node->next`



Memory Controller Design



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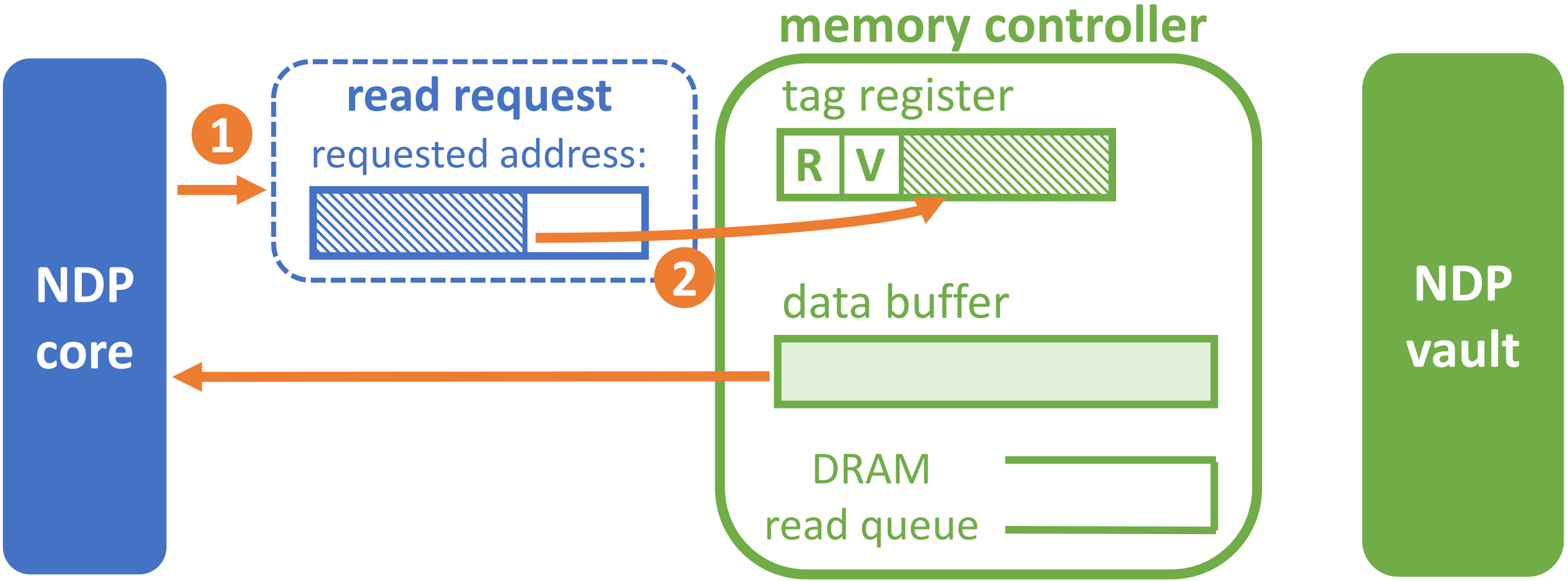

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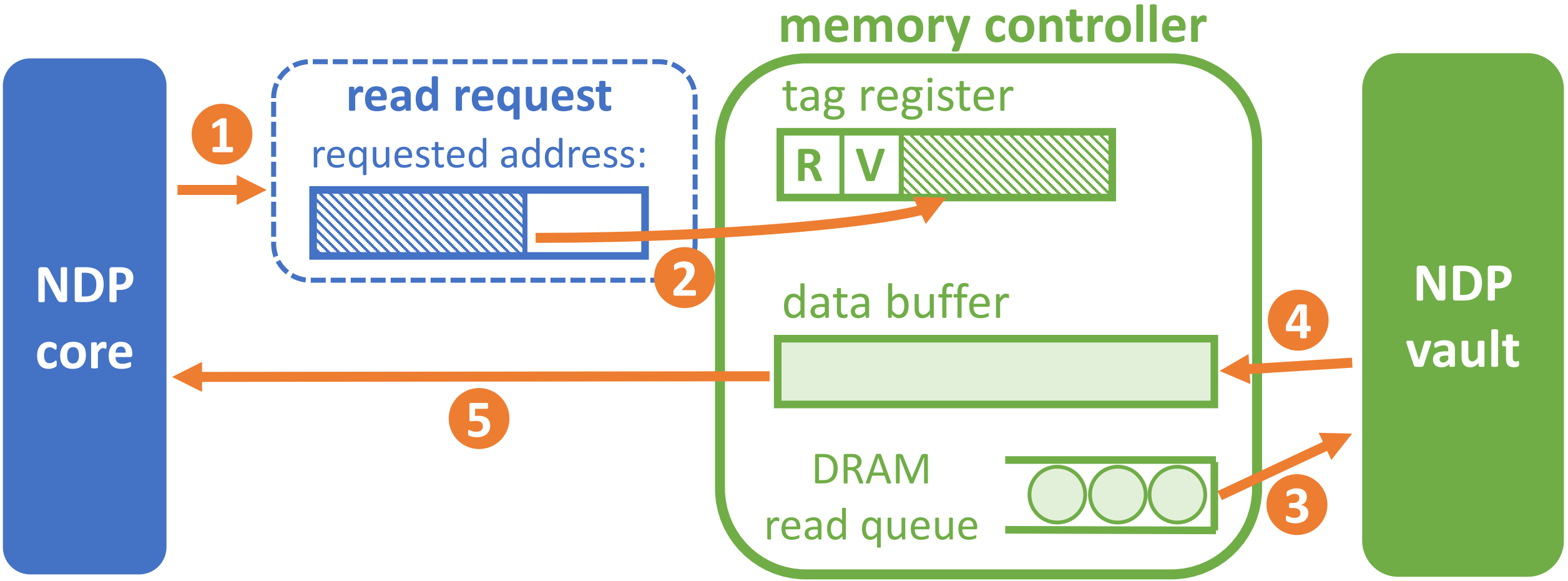

Results

Operation throughput = # data structure operations / second

NDP data buffer compared against:

- **NDP original**: NDP-based implementation w/o hardware change
- **Host FC**: host-based equivalent of NDP-based algorithm
- Host-based state-of-the-art concurrent data structure

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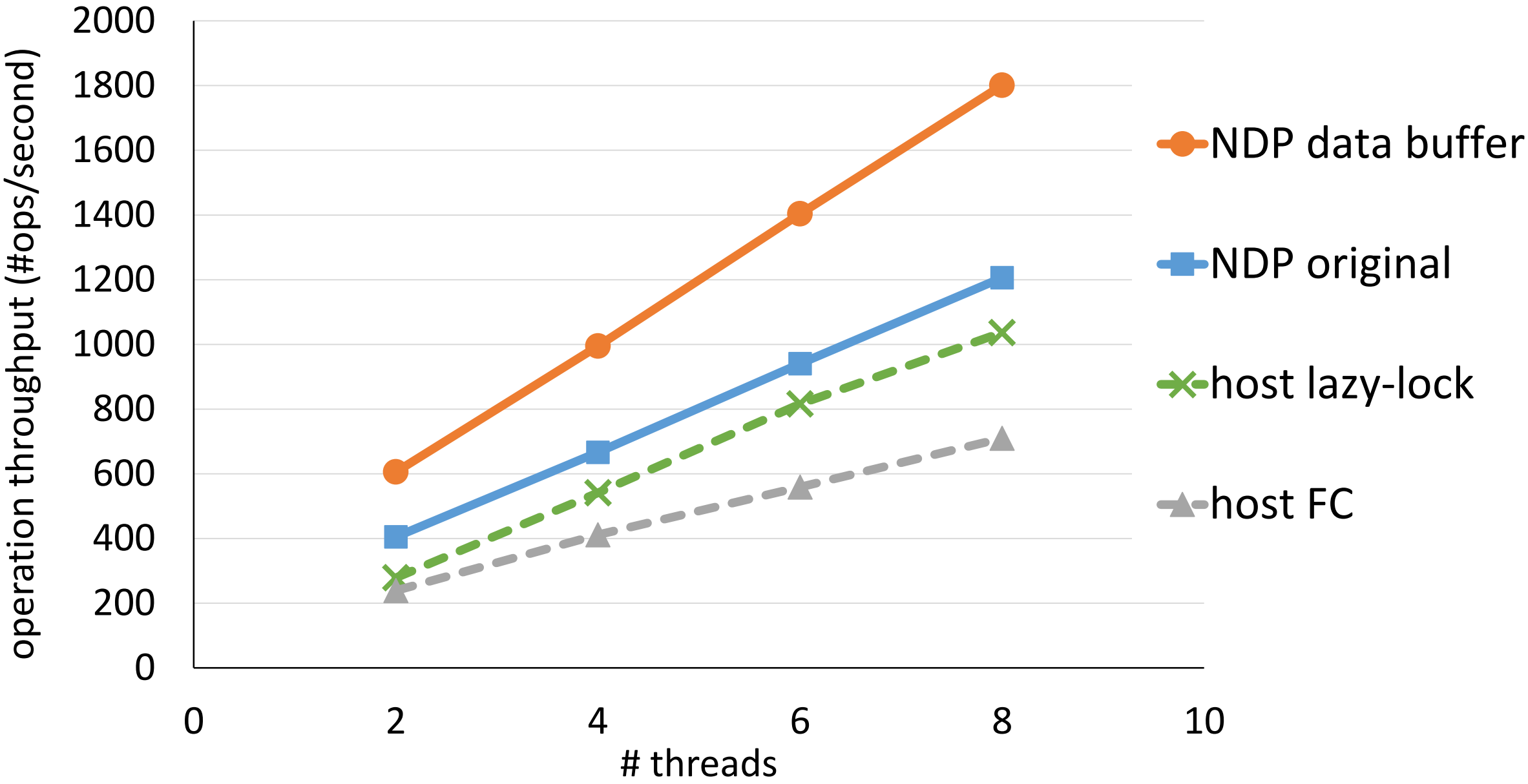

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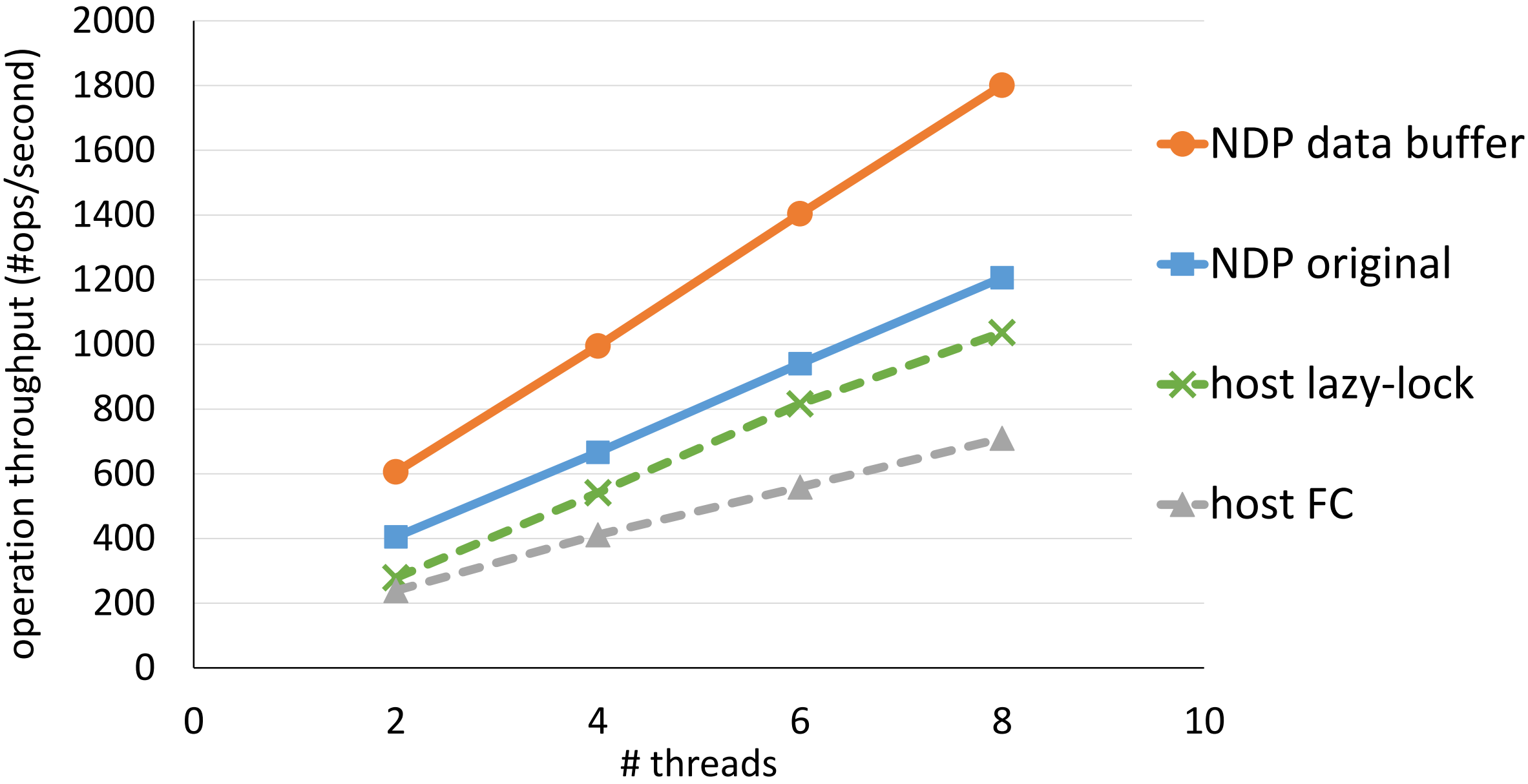

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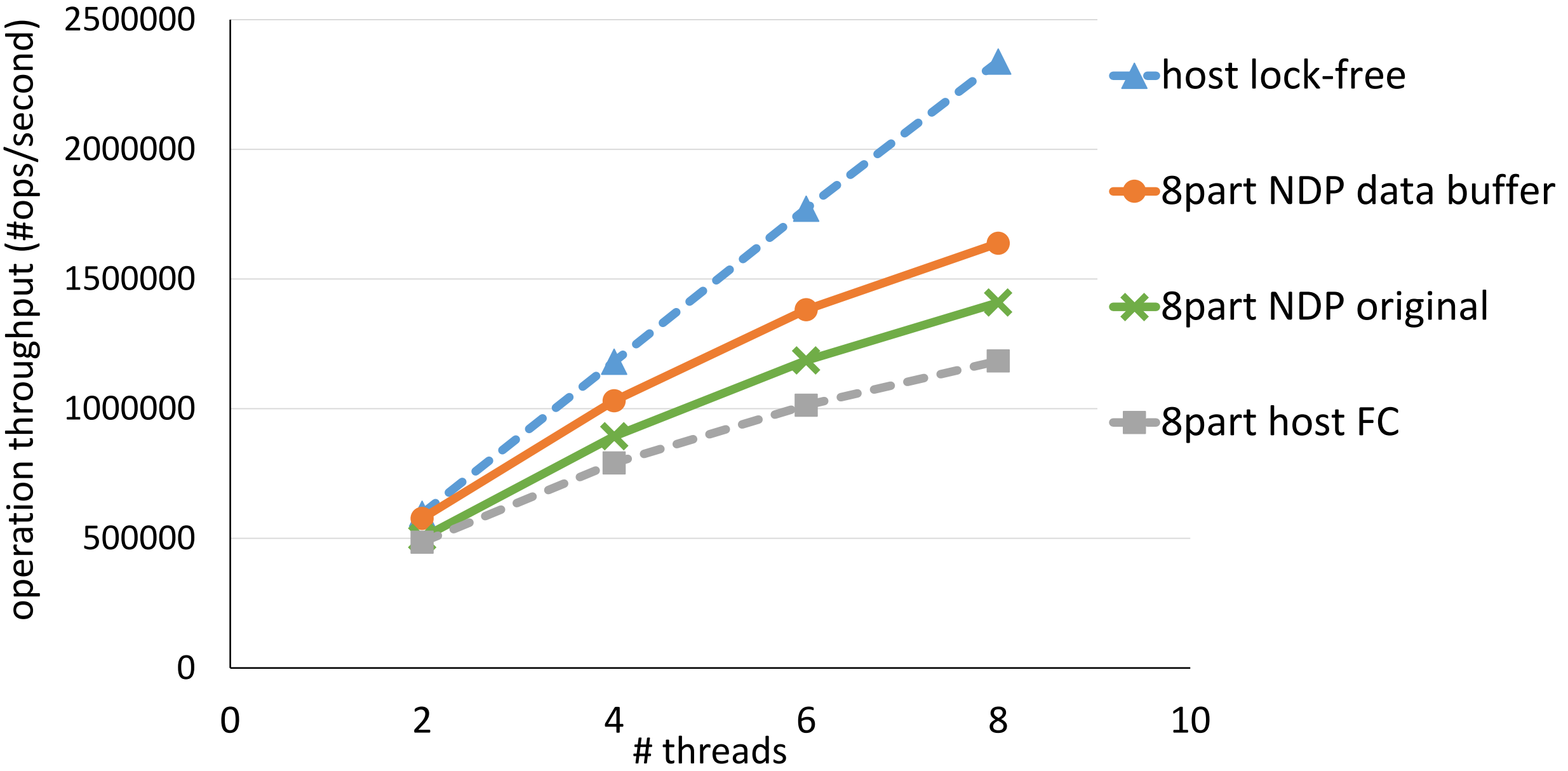

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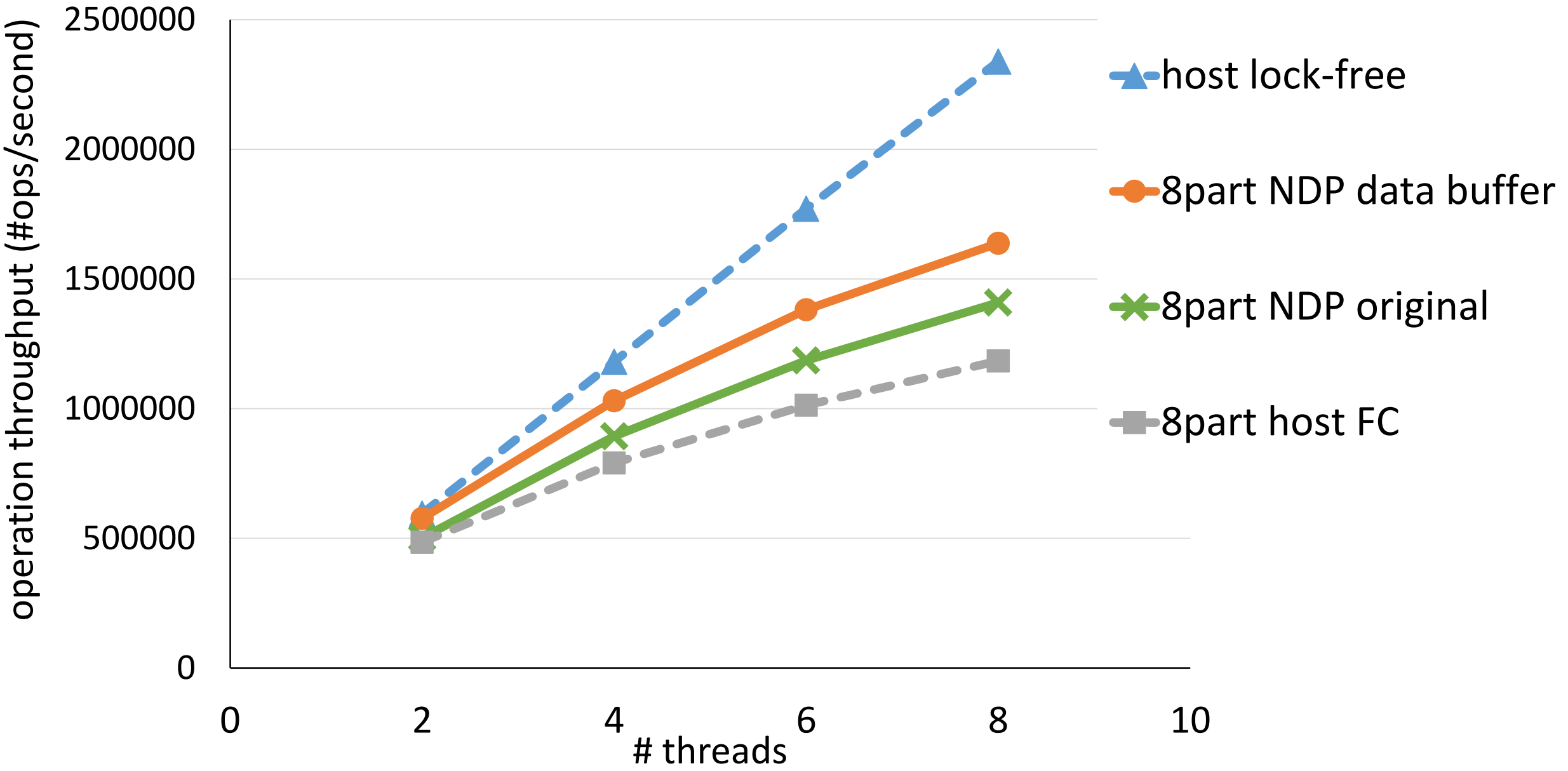

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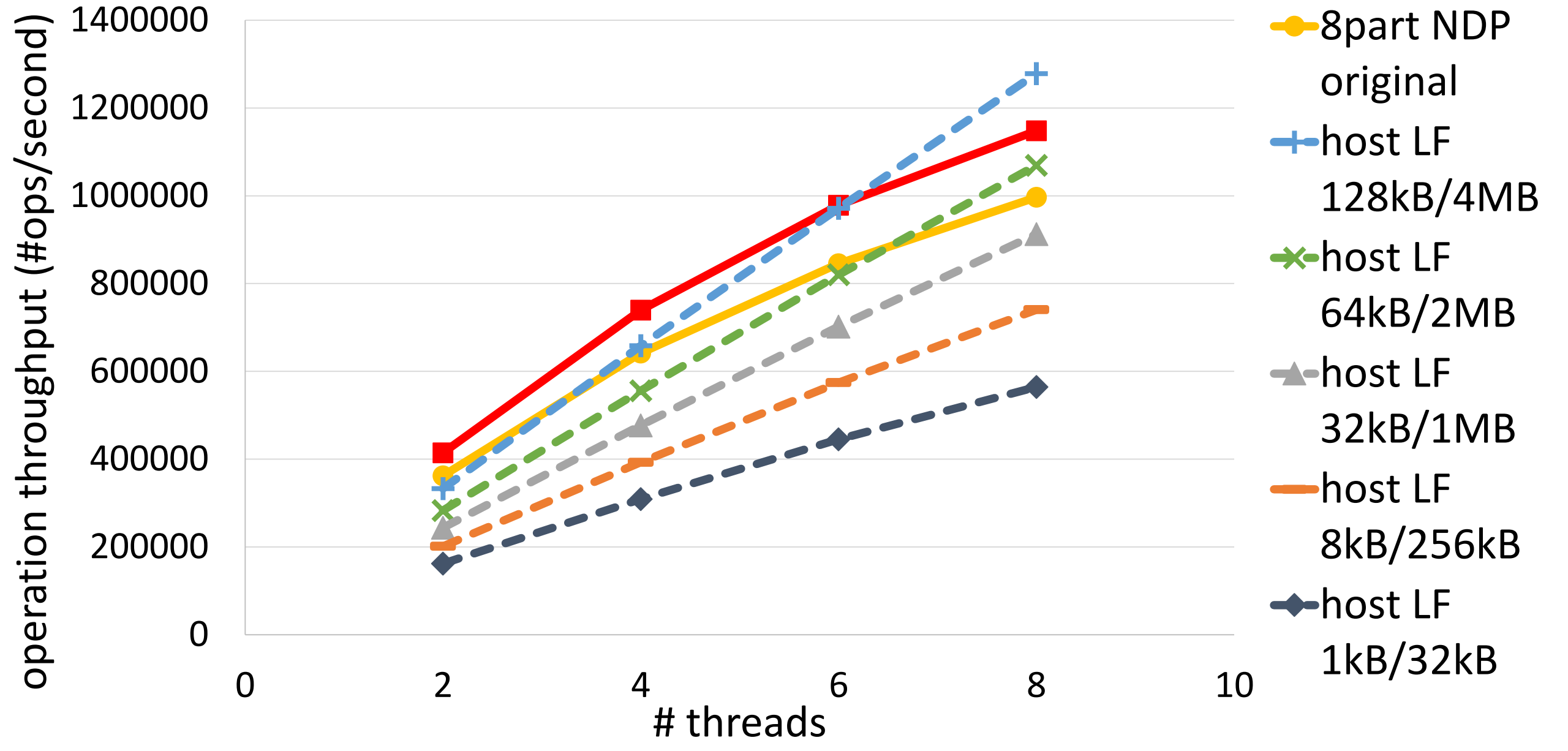
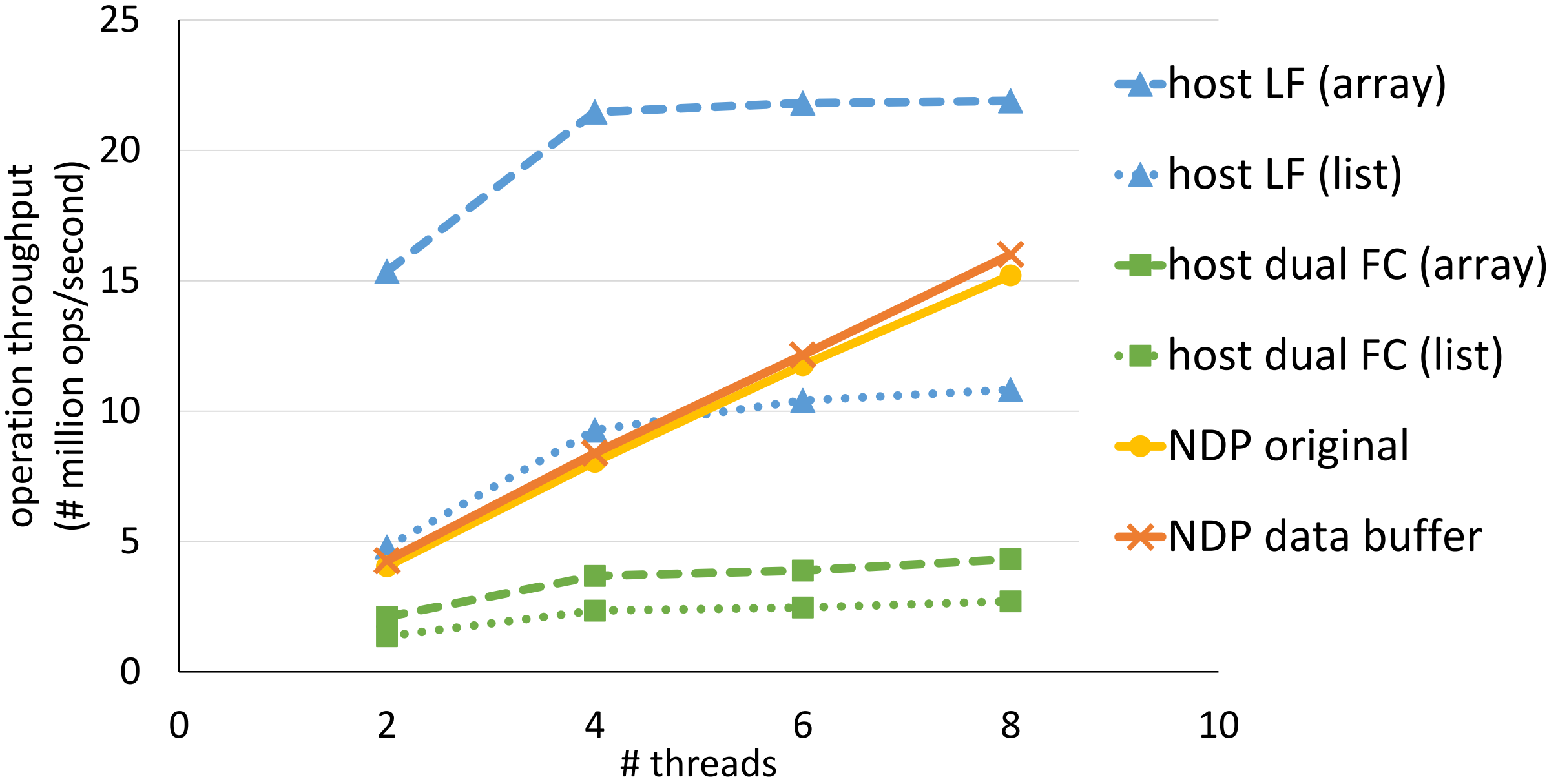


FIFO Queue Results



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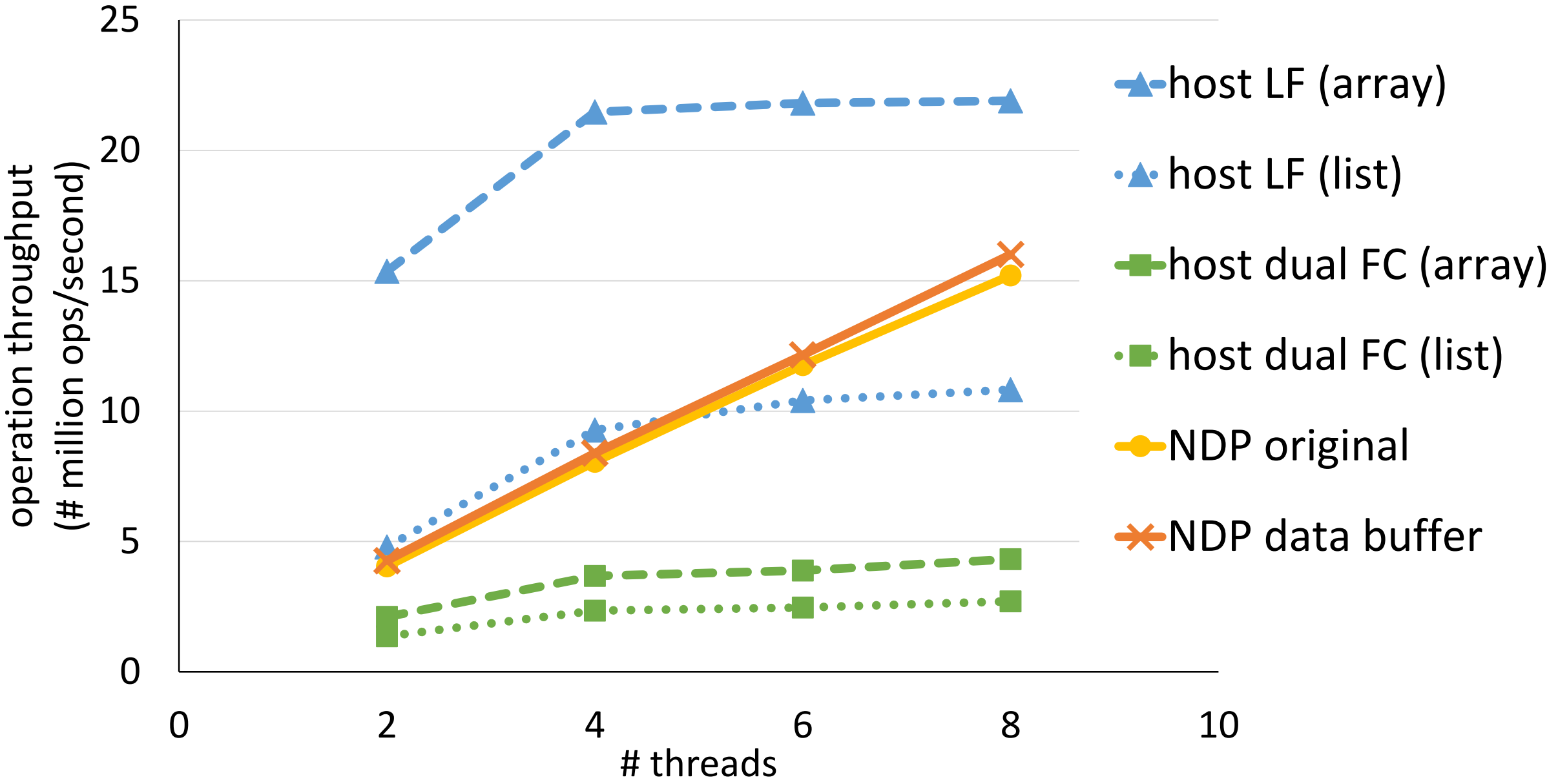

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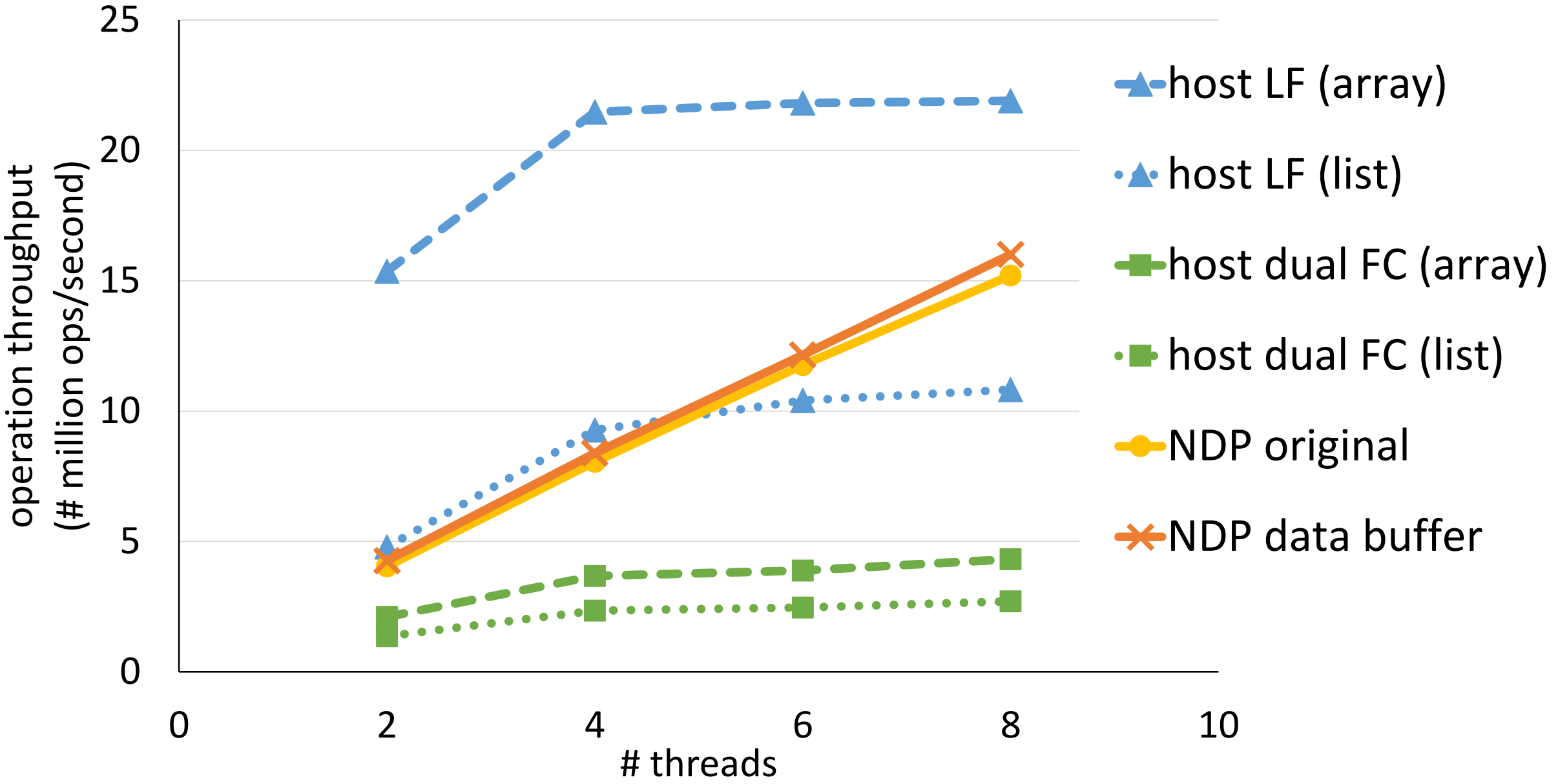

Summary

High performance concurrent data structures w/ NDP

- NDP does not remove DRAM access latencies completely
- Lightweight HW change significantly improves performance
  - Data buffer in memory controller acts as single block cache
  - **Performance improvement compared to w/o data buffer:**
    50% (linked-list), 17% (skiplist), 5% (FIFO queue)